Nanowire Modeling & Design Technical Report

Aidan Prendergast, Claire Ryan Hagar, Imtiaz Ahmed

ajprende@purdue.edu, ryan253@purdue.edu, ahmed202@purdue.edu

PURDUE UNIVERSITY

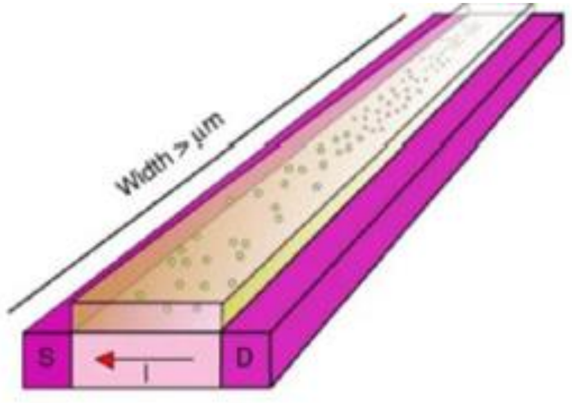
School of Electrical and Computer Engineering

Motivation

- Traditional Planar MOSFET faces several challenges as device dimensions are scaled down.
  - Increased Short channel effects
  - Increased Leakage Currents
  - Deteriorating On/Off Current ratio and Subthreshold Swing
  - Drain-Induced-Barrier-Lowering (DIBL): Drain gets control over Channel conduction

- Continuing Moore's Law—the trend of doubling transistor density approximately every two years- thus becomes more difficult

- Nanowire Transistors provide a nifty way to alleviate these challenges



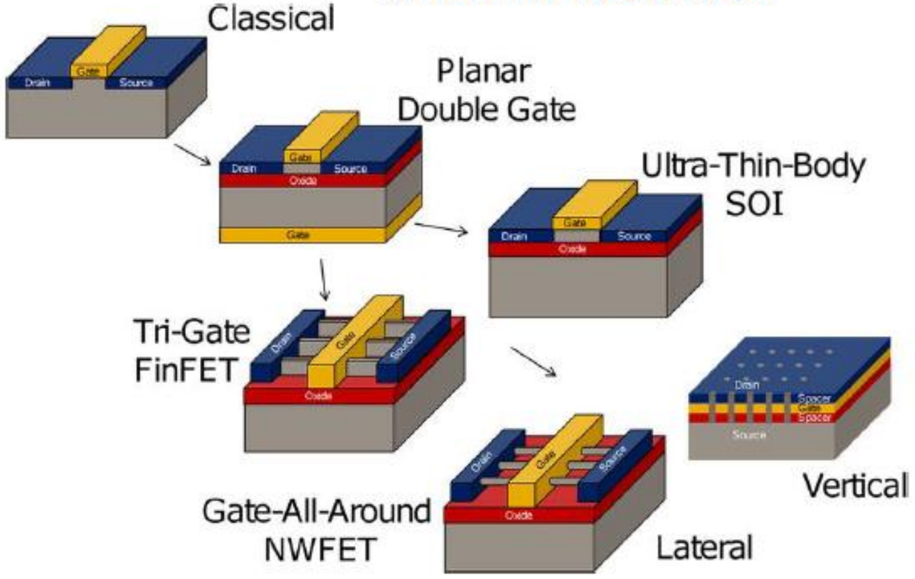
Traditional Planar MOSFET

Motivation

Nanowire Transistors:

- Gate surrounds Channel
- Provides greater Gate control over channel conduction leading to
  - higher switching speeds
  - lower power consumption
  - improved overall performance in terms of On/Off Current ratio and Subthreshold Swing

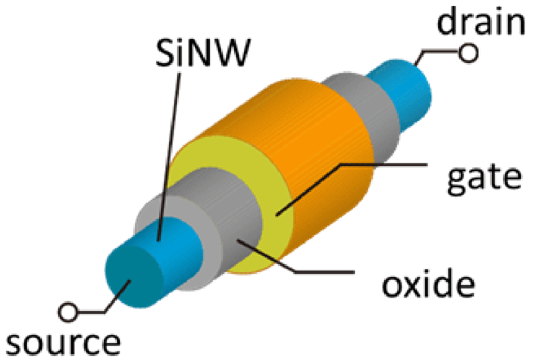
MOSFET Evolution



Goal of this Project:

- Analysis and Comparison of Gate scaling effects in Planar and Nanowire MOSFET
- Analysis of Classical (Drift-Diffusion), Semi-classical (Top-of-the-barrier), and Quantum Transport models of Nanowires
- Exploration of electron and hole nanowire characteristics

Silicon Nanowire



Objective:

- Understand the various physical effects when scaling the gate length of a MOSFET.

Problem:

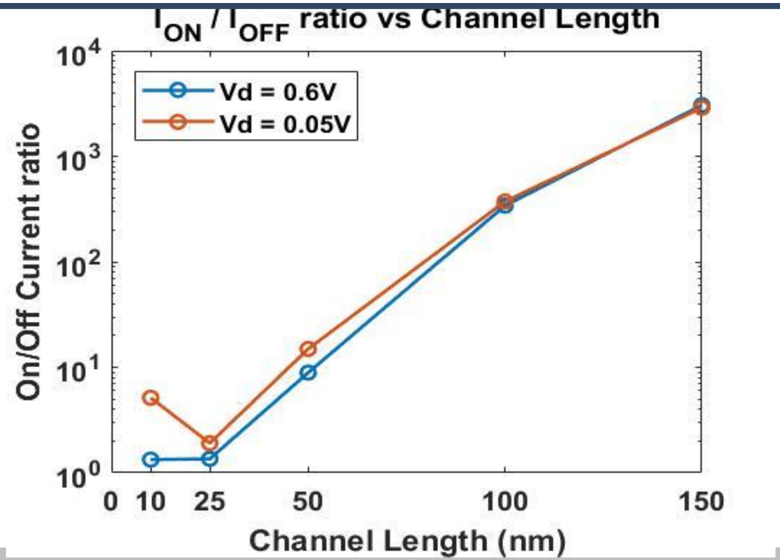
- The ON/OFF current ratio, a large ON current, and the subthreshold swing can all be affected from the gate length.

Results / Impact:

- The ON/OFF current ratio increases as the channel length increase: inverse relationship to subthreshold swing. Also, On Current and Off Current decrease as channel length increases.
- The ON/OFF current ratio is shown below. Others are shown in the Appendix (Transistor Features).
- As we scale the device down, Leakage currents become significant, resulting in high OFF currents and thus deteriorated device performance.

Approach:

- An n-type MOSFET was modeled in NanoHub's MOSFET, varying the gate length from 150nm to 5nm.
- Please see NanoHub MOSFET Inputs (located in the Appendix) for the inputs used in this simulation.



Objective:

- Understand the design changes that can and have been made to increase transistor performance.

Problem:

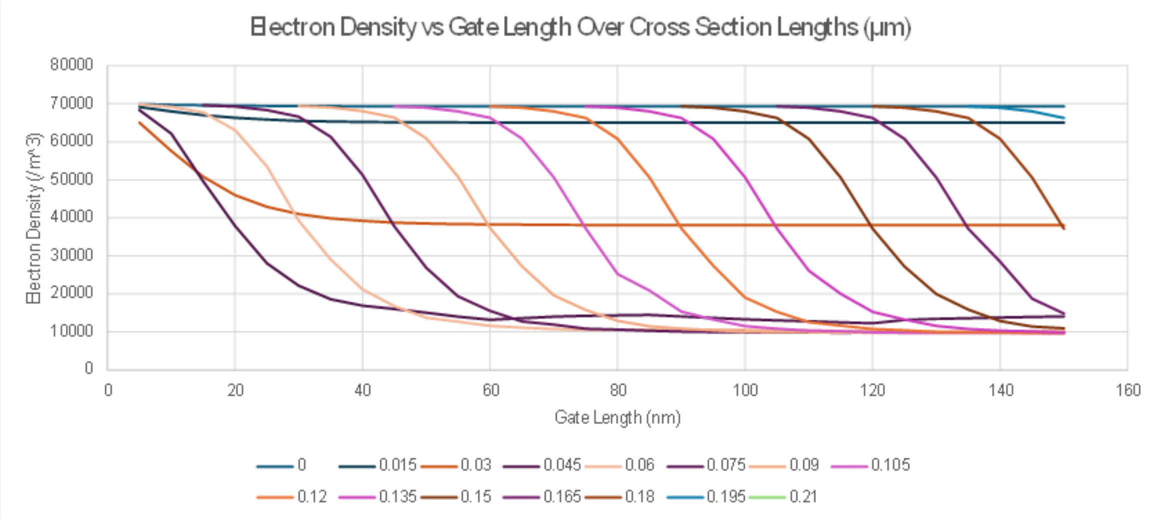
- Various characteristics can be changed to affect the transistor performance.

Results / Impact:

- Both the voltage potential and electron density is decreased with an increase of gate length.
- The relationship of electron density and gate lengths is shown below. Please see Voltage Potentials (located in the Appendix) for the relationship of voltage potential.

Approach:

- An n-type MOSFET was modeled in NanoHub's MOSFET, varying the gate length from 150nm to 5nm.
- Please see NanoHub MOSFET Inputs (located in the Appendix) for the inputs used in this simulation.



Nanowire with Drift Diffusion (Quad Chart 1 of 2)

Objective:

- Understand how critical transistor parameters respond to the scaling of the gate length and nanowire diameter.

Problem:

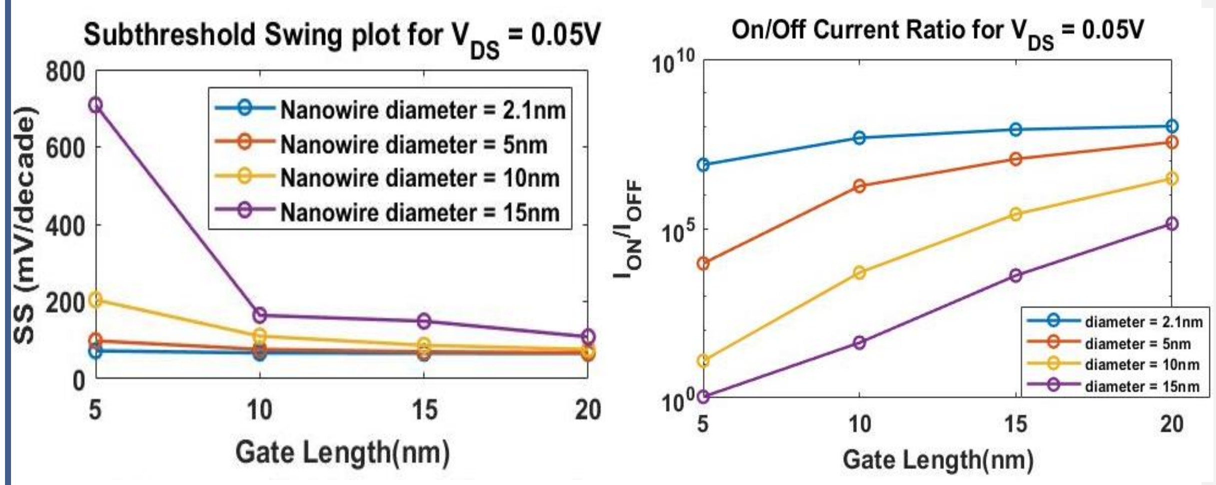
- The ON/OFF current ratio, threshold voltage, and subthreshold swing can all be impacted by changing parameters.

Results / Impact:

- The On/Off current ratio and subthreshold swing improves with decreasing diameter and increasing gate length (figure).
- The threshold voltage increases with increasing gate length and diameter (Appendix - Nanowires with Drift Diffusion: Threshold Voltages).

Approach:

- NanoHub's NANOFINFET tool was used to simulate device performance while varying the nanowire diameter and gate length.
- Please see NANOFINFET Inputs (located in the Appendix) for the inputs used in this simulation.



Nanowire with Drift Diffusion (Quad Chart 2 of 2)

Objective:

- Understand how energy band diagrams vary based on the scaling of the gate length and nanowire diameter.

Problem:

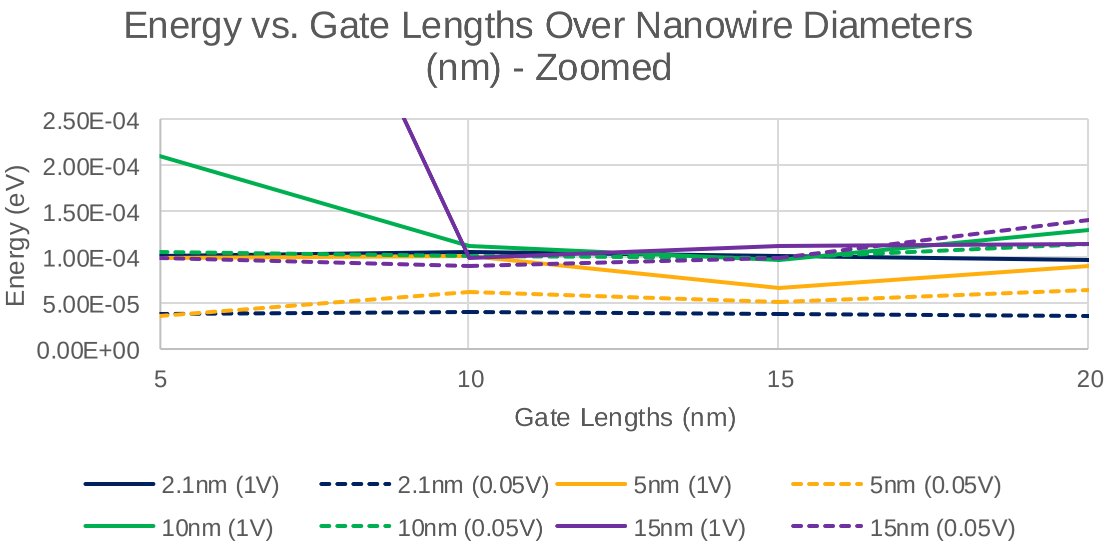
- How does the gate barrier height change as the gate length decreases?

Results / Impact:

- Please see Energy vs. Gate Lengths (located in the Appendix) for more detailed plots.
- Generally, the gate barrier height will increase as the gate length increases. Additionally, a decrease in source-drain voltage will result in a decrease of energy.

Approach:

- NanoHub's NANOFINFET tool was used to simulate device performance while varying the nanowire diameter and gate length.
- Please see NANOFINFET Inputs (located in the Appendix) for the inputs used in this simulation.



Objective:

- Understand workfunctions

Problem:

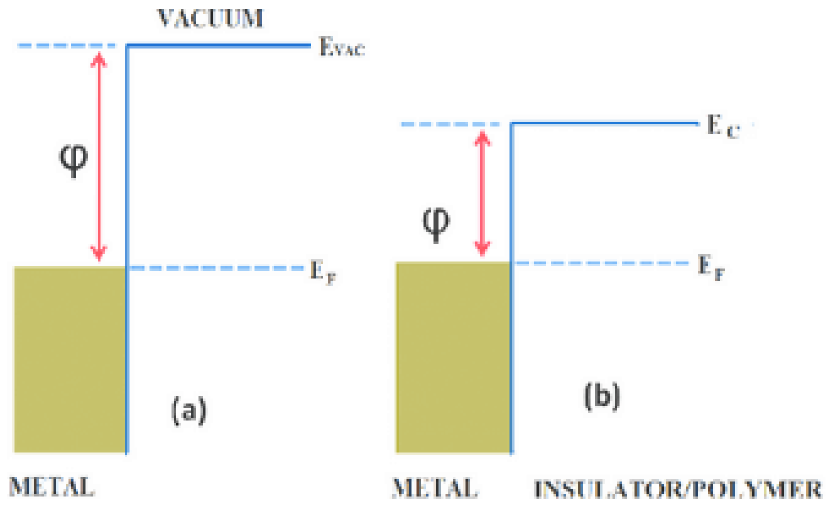
- What is the physics of "workfunction"?
- What are reasonable experimental values of workfunction?

Results / Impact:

- Workfunction is the minimum energy required to move an electron to a place away from the surface, but still close enough to be impacted be the surface’s electric field. (see [1])
- For silicon, reasonable workfunction values range from 4.60 – 4.85 eV. (see [1])

Approach:

- The term workfunction was researched online to gain an understanding of its physics.



[1]

Nanowire with Drift Diffusion – Workfunction Variations and Gate Potential Analysis (Quad Chart 2 of 2)

Objective:

- Understand how a long vs short gate length nanowire effects the I-V characteristics.

Problem:

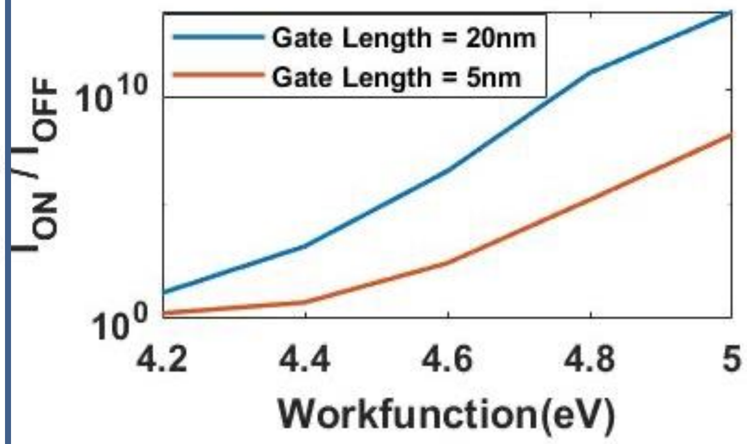
- The ON/OFF current ratio, threshold voltage, and subthreshold swing can all be impacted by changing parameters.

Results / Impact:

- As workfunction increases, the on/off current ratio increases (figure), and subthreshold swing decreases (appendix) as a result.
- Normalization of I-V data by choosing a workfunction is often done for getting rid of device-to-device variation when performing comparison
- Please see Transistor Parameters in the Appendix for additional plots.

Approach:

- NanoHub's NANOFINFET tool was used to simulate device performance while varying the gate contact workfunction.
- Please see NANOFINFET Inputs (located in the Appendix) for the inputs used in this simulation.



Smaller Gate device with low workfunction
⟹ barrier too low
⟹ higher I_{OFF}

Objective:

- Understand the relationship between electron masses and nanowires.

Problem:

- As the electron masses of Silicon change from 0.91 to 0.19, what do the wavefunctions and eigen energies mean for nanowire?

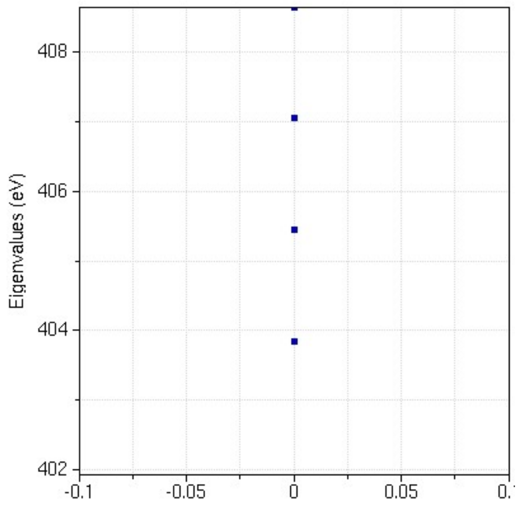
Results / Impact:

- The wavefunctions do not demonstrate a significant difference between electron masses.
- The eigen energies of a greater electron mass show lower energies, and a tighter grouping of energies (see below). As the energies get closer, forming one overlapping energy, the nanowire will lose the 1-D characteristics.

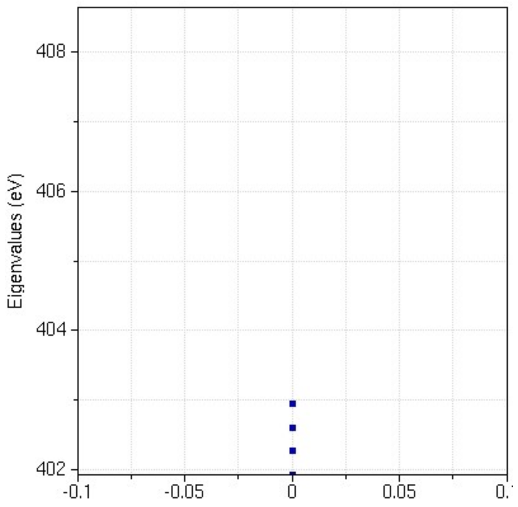
Approach:

- A flat Cylinder with heigh of 1nm was modeled in QuantumDotLab, varying the effective mass from 0.91 to 0.19.
- Please see NanoHub Quantum Dot Lab Inputs (located in the Appendix) for the inputs used in this simulation.

Effective Mass: 0.19



Effective Mass: 0.91



Objective:

- Compare the I-Vg curves between difference crystal directions of Silicon.

Problem:

- What is the difference in I-Vg curves between 100, 110, and 111 crystal directions?

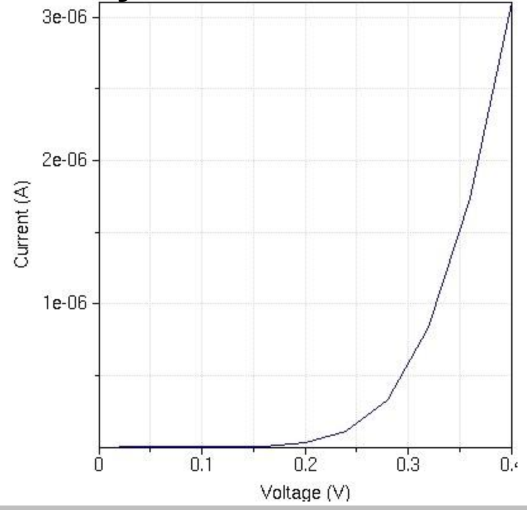
Results / Impact:

- Shown below is the comparison of 110 and 111 crystal directions. The I-Vg curve of 100 does not exist.
- Shown in 1D Electron Densities and 3D Electron Densities (located in the Appendix) are the comparisons of the electron densities. They are very similar between crystal directions.

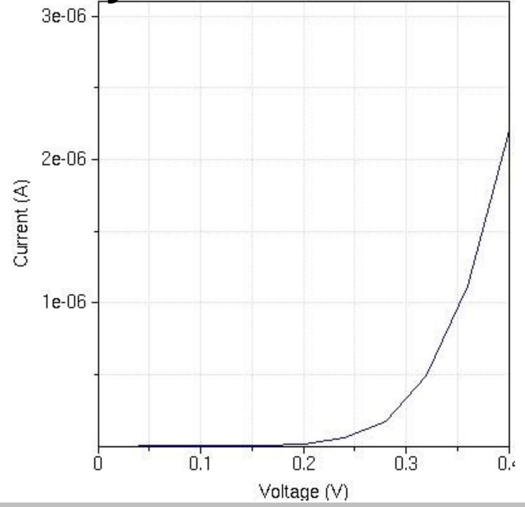
Approach:

- A silicon nanowire of diameter 2nm was modeled in Nanowire, varying the crystal direction.
- Please see NanoHub Nanowire Inputs (located in the Appendix) for the inputs used in this simulation.

Crystal Direction: 110



Crystal Direction: 111



Nanowire Realistic Bandstructure (Quad Chart 1 of 2)

Objective:

- Understand the bandstructure of a nanowire.

Problem:

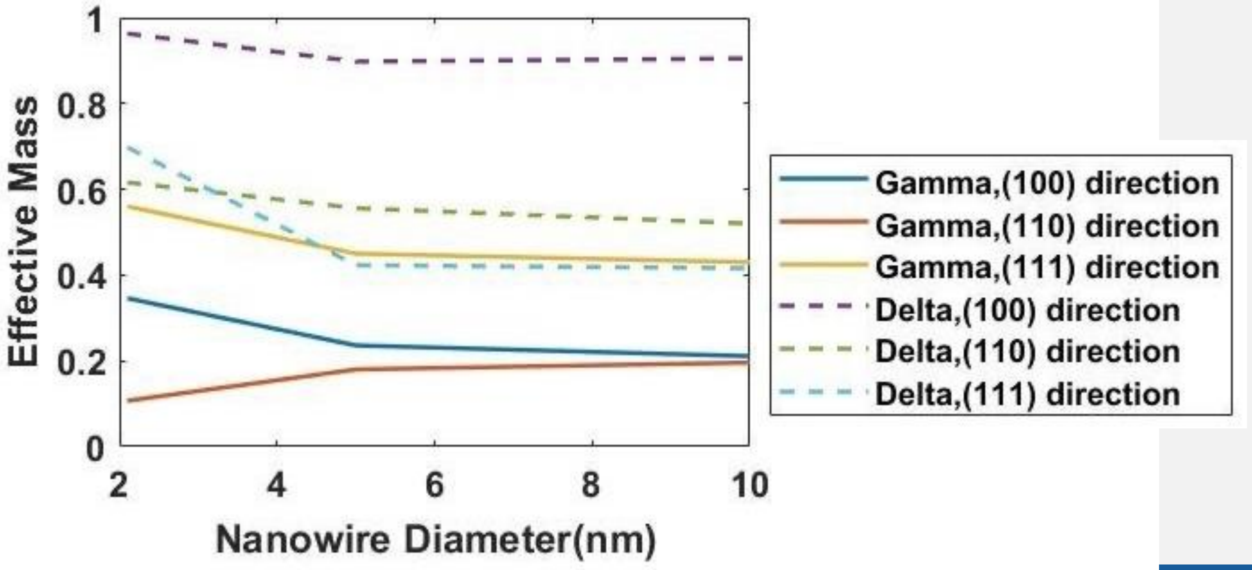
- How does the mass at the different points in a nanowire vary with diameter and transport directions?

Results / Impact:

- The mass is greater at the Delta line (when k>0) than at the Gamma point (when k=0).
- Generally, the mass will decrease as the nanowire diameter increases.
- Please see Nanowire Realistic Bandstructure (Masses) (in the Appendix) for more detailed plots.

Approach:

- A silicon nanowire was modeled in NanoHub's BandstructureLab, varying the nanowire transport direction and diameter.
- Please see NanoHub BandstructureLab Inputs (located in the Appendix) for the inputs used in this simulation.



Objective:

- Understand the bandstructure of a nanowire.

Problem:

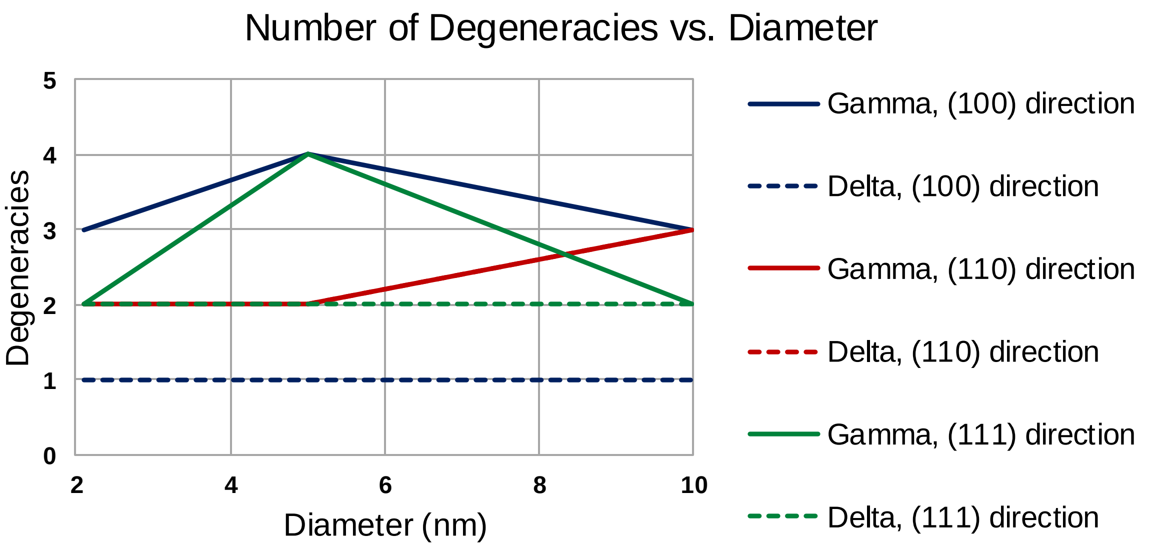
- How does the degeneracies at the different points in a nanowire vary with diameter and transport directions?

Results / Impact:

- For 100 and 111 transport directions, there are more degeneracies at the Gamma point.
- The number of degeneracies vary in no significant pattern based on nanowire diameter.
- Please see Nanowire Realistic Bandstructure (Degeneracies) (in the Appendix) for more detailed plots and detailed data Table

Approach:

- A silicon nanowire was modeled in NanoHub's BandstructureLab, varying the nanowire transport direction and diameter.
- Please see NanoHub BandstructureLab Inputs (located in the Appendix) for the inputs used in this simulation.



Nanowire Top-of-Barrier Transport (Quad Chart 1 of 2)

Objective:

- Understand electron transport through nanowires.

Problem:

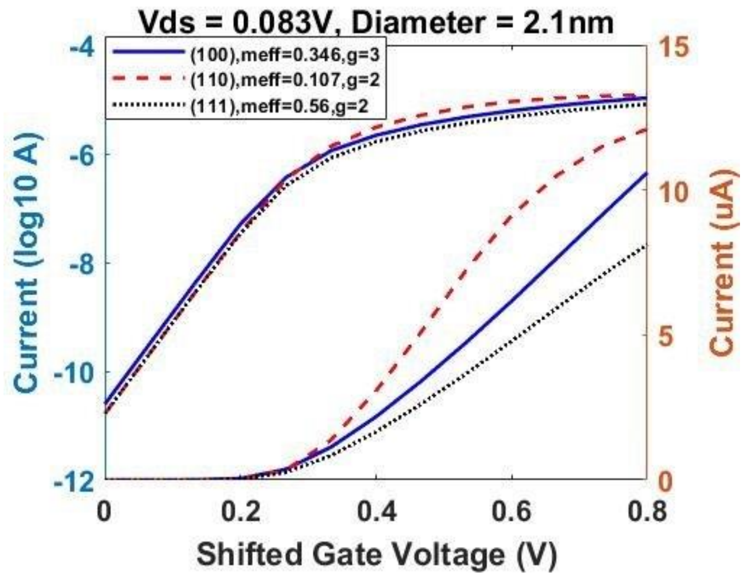
- How does the I-V curve differ between nanowire transport directions (100, 110, and 111) and differing diameters (2.1nm and 10nm)?

Results / Impact:

- The currents are generally largest in the 110 direction and smallest in the 111 direction.
- The currents increase with an increase in nanowire diameter.
- Please see Nanowire Top-of-Barrier Transport (I-V Curves) for both plots.

Approach:

- A silicon nanowire was modeled in NanoHub's FETtoy tool, varying the nanowire transport direction and diameter. The masses and degeneracies from Challenge #5 were also utilized (please see inputs).
- Please see NanoHub FETtoy Inputs (in the Appendix) for the inputs used in this simulation.



Objective:

- Understand electron transport through nanowires.

Problem:

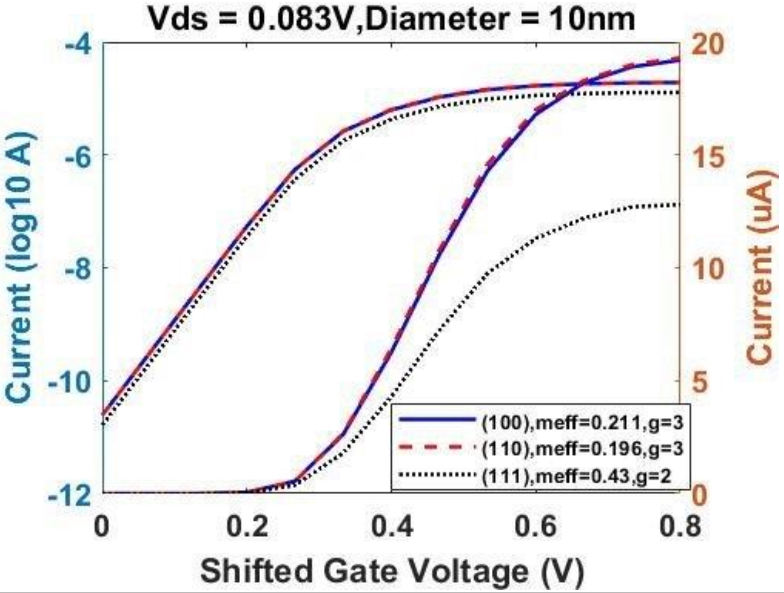
- How do the inputs alphaG and alphaD relate realistic capacitances?

Results / Impact:

- alphaG and alphaD quantities refer to Gate and Drain control parameter respectively.
- Ideally the Gate must have complete control over the channel and not drain. However, due to Drain Induced Barrier Lowering (DIBL), transistor sees a lowering of threshold voltage, mostly in short channel devices.
- Results in Drain control over Channel.

Approach:

- A silicon nanowire was modeled in NanoHub's FETtoy tool, varying the nanowire transport direction and diameter. The masses and degeneracies from Challenge #5 were also utilized (please see inputs).
- Please see NanoHub FETtoy Inputs (in the Appendix) for the inputs used in this simulation.



$$\alpha_G = \frac{C_G}{C_G + C_D + C_S}$$

$$\alpha_D = \frac{C_D}{C_G + C_D + C_S}$$

Fast Nanowire Quantum Transport

Objective:

- Explore Fully Quantum Mechanical Transport Calculation

Problem:

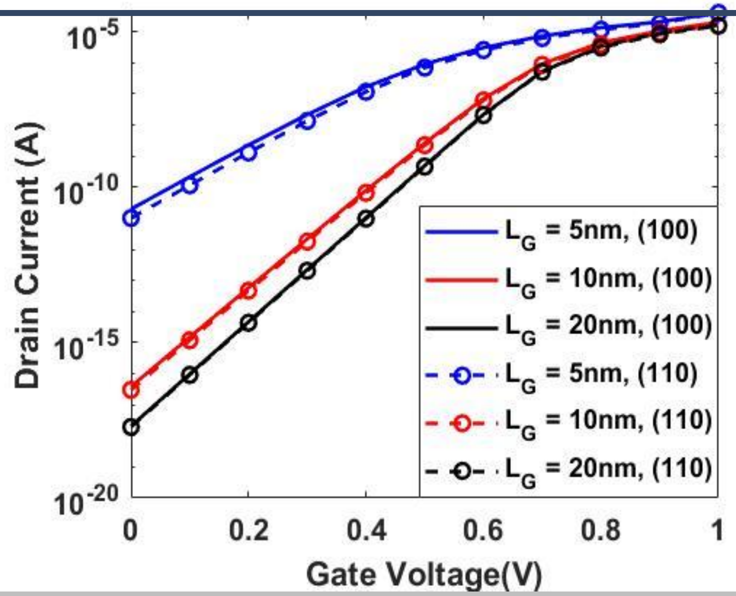
- Modeling 3nm Gate-all-around nanowires

Results / Impact:

- Gate-all-around nanowire provides better electrostatic gate control over channel
- Even for a Gate Length as short as 5nm, Off current is significantly low ⟹ better I_{ON}/I_{OFF}
- Charge profiles across Gate lengths and Crystal direction shown in Appendix (Charge Density Profiles)

Approach:

- 3nm Gate-all-around nanowires were modeled using Multi-gate Nanowire FET tool on nanoHub.
- Effects of varying Gate length (5nm, 10nm, 20nm) in 2 different crystal directions studied



Long Nanowire Quantum Transport (Quad Chart 1 of 2)

Objective:

- Understand atomistic quantum transport through 2.1nm cross section nanowires using a gate and channel length of 15nm.

Problem:

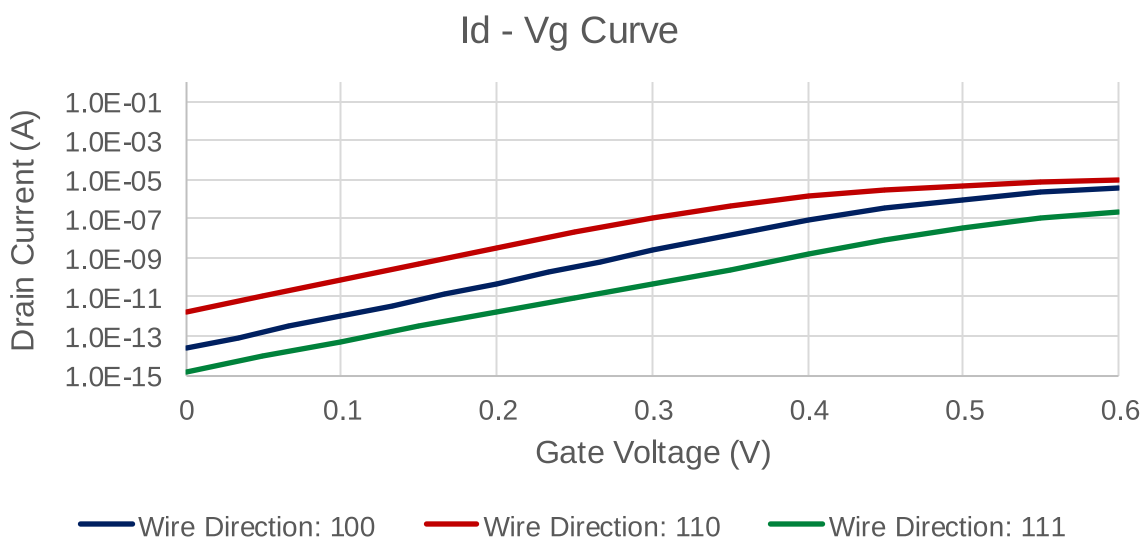
- What are the general features of the I-V curves of 100, 110, and 111 wire directions?

Results / Impact:

- Shown below on the logarithmic plot, the drain current is the greatest in the 110 direction and lowest in the 111 direction.
- All directions start to slow their increase in current between 0.35V and 0.55V.

Approach:

- A silicon nanowire was modeled in NanoHub's Omenwire tool, varying the nanowire transport direction.
- Please see NanoHub Inputs (located in the Appendix) for the inputs used in this simulation.



Long Nanowire Quantum Transport (Quad Chart 2 of 2)

Objective:

- Understand atomistic quantum transport through 2.1nm cross section nanowires using a gate and channel length of 15nm.

Problem:

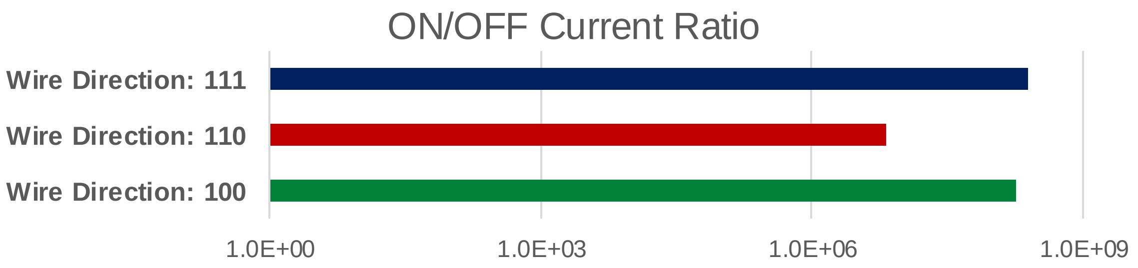
- How do the subthreshold swings and On/Off current ratios differ between 100, 110, and 111 wire directions?

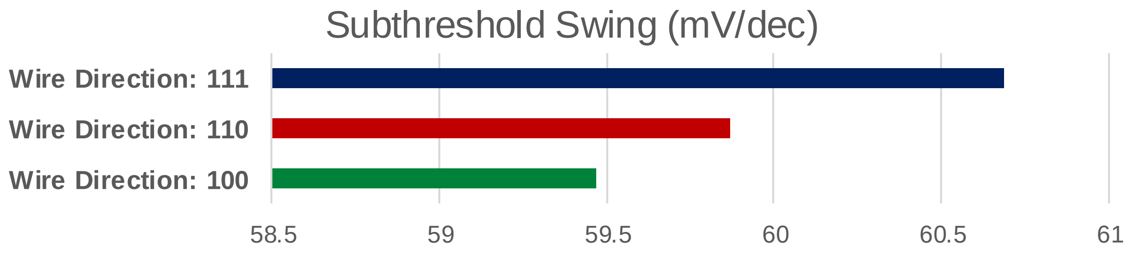
Results / Impact:

- The On/Off current ratio in the 110 direction is drastically smaller than the others.
- The subthreshold swing however has a linear change between the 100, 110, and 111 direction, steadily increasing.

Approach:

- A silicon nanowire was modeled in NanoHub's Omenwire tool, varying the nanowire transport direction.
- Please see NanoHub Inputs (located in the Appendix) for the inputs used in this simulation.





Objective:

- Understand atomistic quantum transport through 1.9nm cross section nanowires using a gate and channel length of 5nm.

Problem:

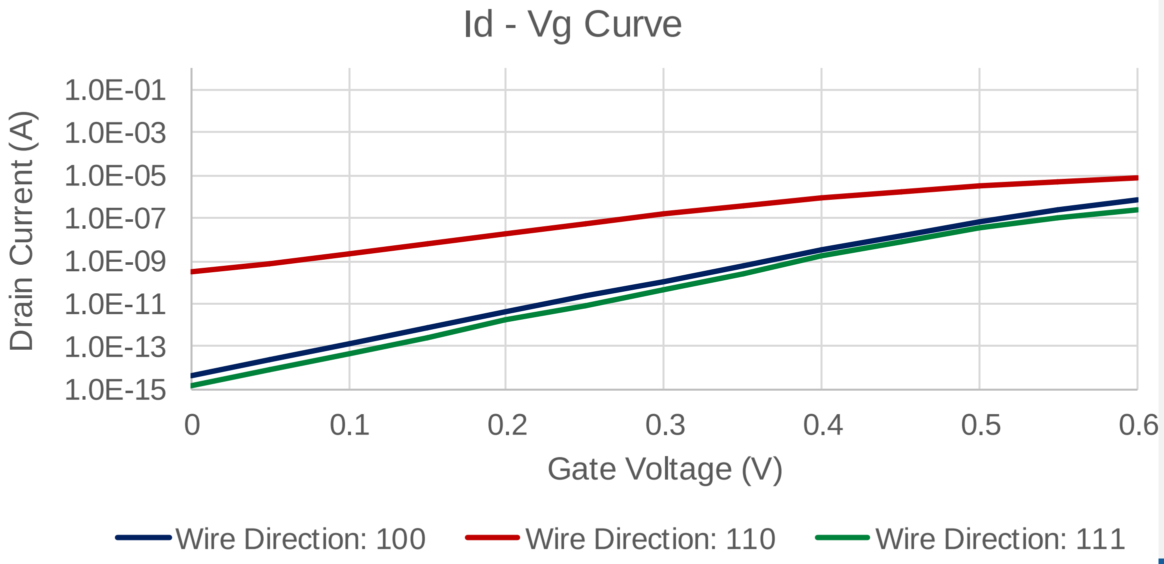
- What are the general features of the I-V curves of 100, 110, and 111 wire directions?

Results / Impact:

- Shown below on the logarithmic plot, the drain current is the greatest in the 110 direction and lowest in the 111 direction.
- The current is very similar in the 100 and 111 directions.
- All directions don't start to slow their increase in current until after 0.55V.

Approach:

- A silicon nanowire was modeled in NanoHub's Omenwire tool, varying the nanowire transport direction.
- Please see NanoHub Inputs (located in the Appendix) for the inputs used in this simulation.



Aidan Prendergast, Claire Ryan Hagar, Imtiaz Ahmed

Short Nanowire Quantum Transport (Quad Chart 2 of 2)

Objective:

- Understand atomistic quantum transport through 1.9nm cross section nanowires using a gate and channel length of 5nm.

Problem:

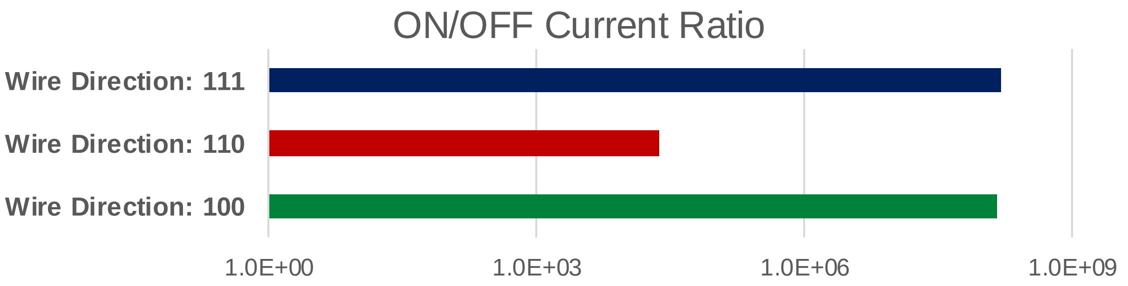
- How do the subthreshold swings and On/Off current ratios differ between 100, 110, and 111 wire directions?

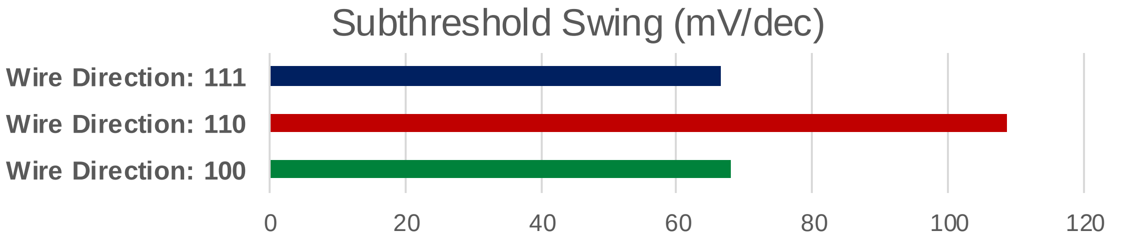
Results / Impact:

- The On/Off current ratio did not significantly change between the long and short nanowire.
- The subthreshold swing did show a large difference. With the short nanowire, the 110 direction showed a large increase.

Approach:

- A silicon nanowire was modeled in NanoHub's Omenwire tool, varying the nanowire transport direction.
- Please see NanoHub Inputs (located in the Appendix) for the inputs used in this simulation.





Objective:

- Understand what inputs can be used to increase the performance of a nanowire.

Problem:

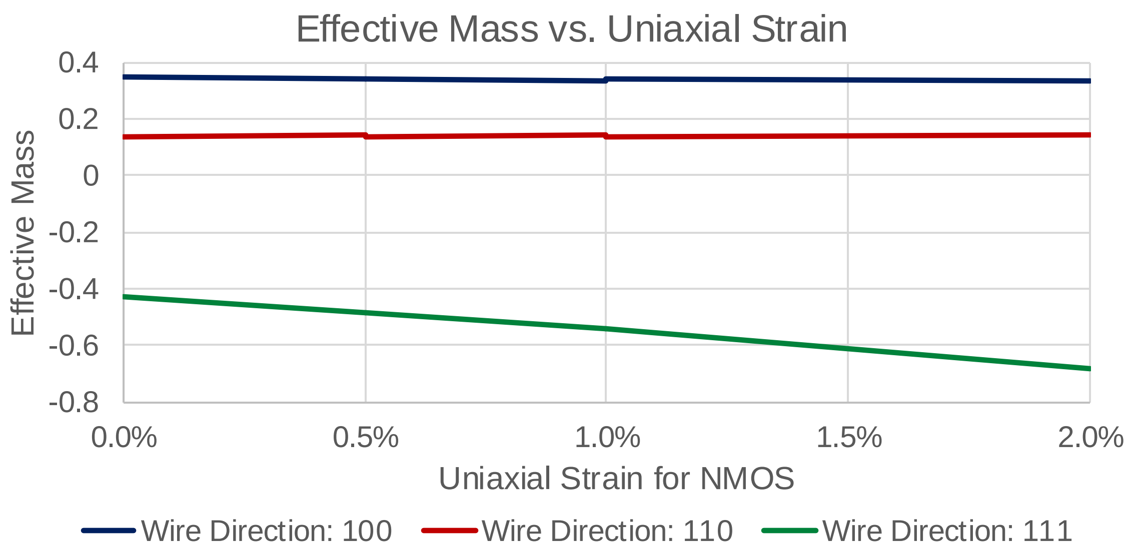
- How can the nanowire be tuned to better the transistor performance?

Results / Impact:

- The effective mass (m*) is defined as the inverse of the second derivate of E-k times the square of Plank's constant.
- m* varies inversely with the sharpness, or curvature, of the bands. This is decreased by increasing the strain (shown below).

Approach:

- A silicon nanowire was modeled in NanoHub's BandstructureLab tool, varying the uniaxial strain from 0%, 0.5%, 1%, & 2%.
- Please see NanoHub Inputs (located in the Appendix) for the inputs used in this simulation.



Objective:

- Understand what inputs can be used to increase the performance of a nanowire.

Problem:

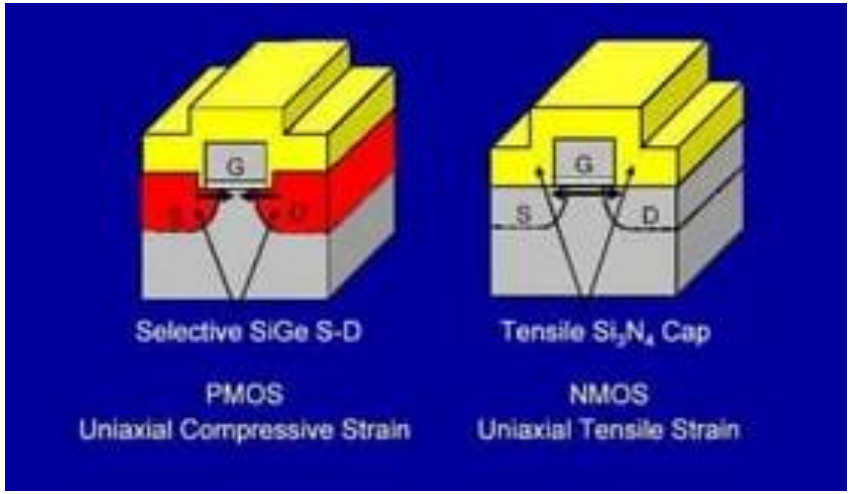
- What kinds of strain is associated with transistors? What is reasonable to do with nanowires?

Approach:

- Various publications were researched for what kind of strain is associated with transistors.
- Please see Resources 2 – 5 (located in the Appendix) for the list of publications reviewed.

Results / Impact:

- Each publication reviewed concluded that NMOS transistors should be stretched to enhance electron mobility.
    - PMOS transistors should be compressed to enhance hole mobility.
- Also noted, using two separate crystal directions would be most optimal, but it is not realistic outside of a simulation.



[3]

Objective:

- Understand how changes to a transistor impact performance.

Problem:

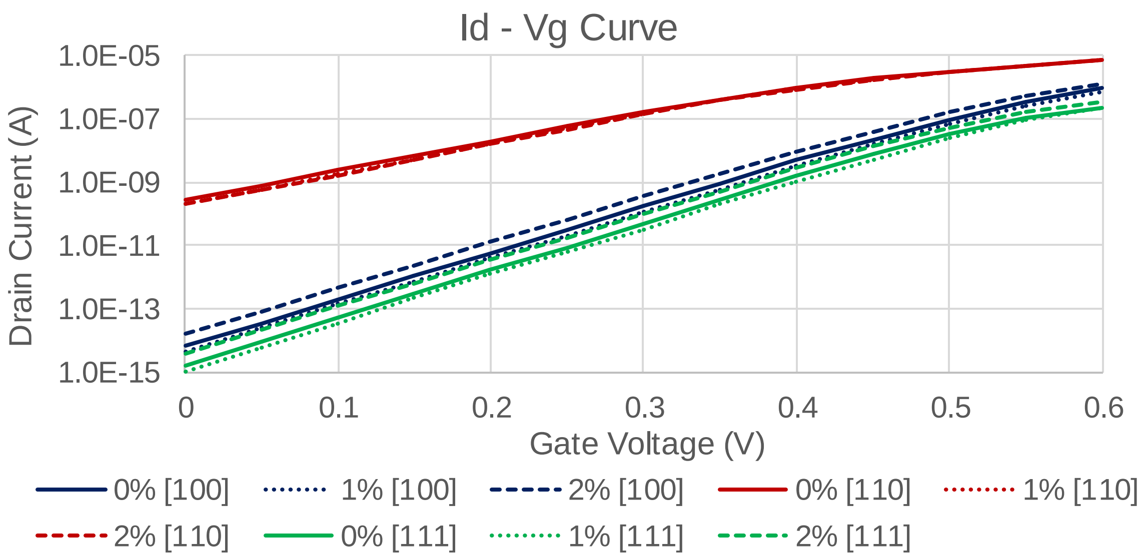
- How did the changes implemented in Challenge #10 impact the performance of the transistor?

Results / Impact:

- Shown below and in Id-Vg Curve (located in the Appendix) in greater detail, there is not a significant difference between the I-V curves for various uniaxial strains.

Approach:

- A silicon nanowire was modeled in NanoHub's Omenwire tool, varying the uniaxial strain from 0%, 1%, & 2%.
- Please see NanoHub Inputs (located in the Appendix) for the inputs used in this simulation.



Optimized Nanowire Quantum Transport (Quad Chart 2 of 2)

Objective:

- Understand how changes to a transistor impact performance.

Problem:

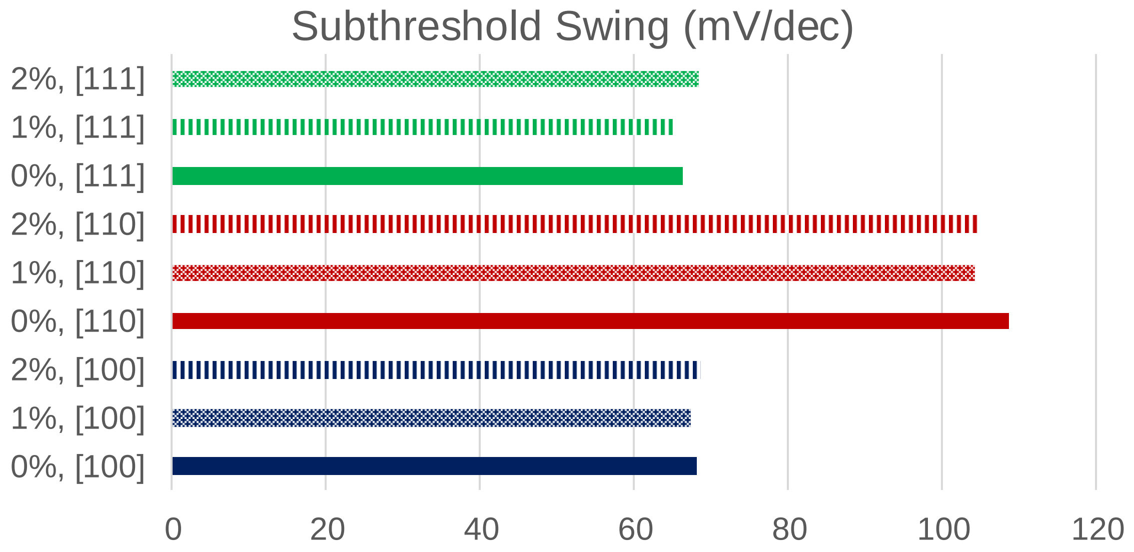
- What other improvements could be made to better the performance?

Results / Impact:

- The subthreshold swing (shown below) and the on/off current ratio (shown in the Appendix, Critical Parameters) demonstrate the best performance will occur at 1% strain (compared to 0% or 2%).

Approach:

- A silicon nanowire was modeled in NanoHub's Omenwire tool, varying the uniaxial strain from 0%, 1%, & 2%.
- Please see NanoHub Inputs (located in the Appendix) for the inputs used in this simulation.



Hole Nanowire Bandstructure (Quad Chart 1 of 2)

Objective:

- Understand the hole bandstructure in nanowires.

Problem:

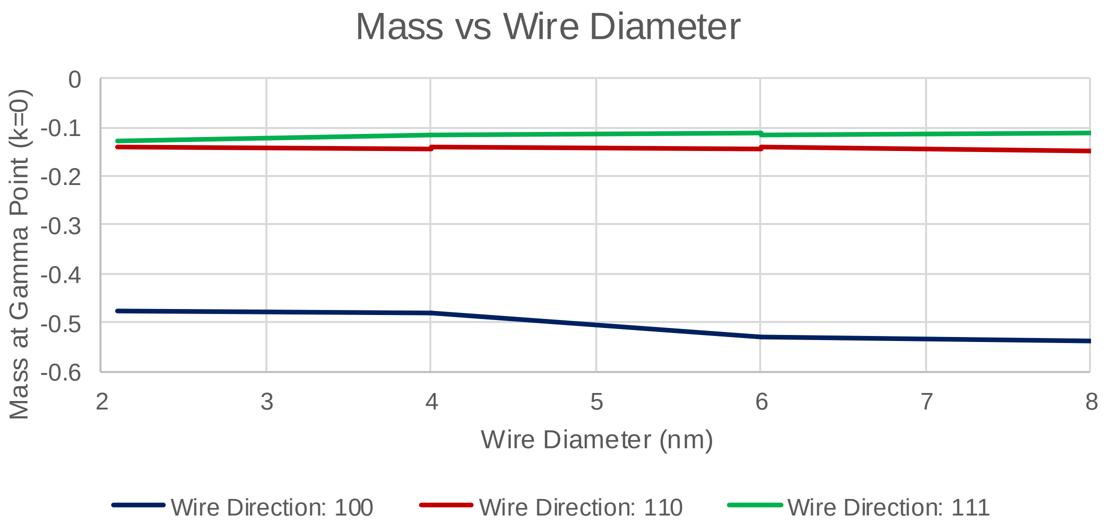
- How does the mass at Gamma Point (k=0) change as a function of the wire diameter?

Results / Impact:

- Shown below, for wire directions 110 and 111, the mass at the Gamma point does not have a significant change.
- For wire direction 100, the mass decreases at the Gamma point.
  - There are peaks off the Gamma point of -0.524, -0.722, and -0.518 for 2.1nm, 4nm, and 6nm diameters respectively.

Approach:

- A silicon nanowire was modeled in NanoHub's BandstructureLab tool, varying the wire diameter from 2.1nm, 4nm, 6nm, and 8nm.
- Please see NanoHub Inputs (located in the Appendix) for the inputs used in this simulation.



Hole Nanowire Bandstructure (Quad Chart 2 of 2)

Objective:

- Understand the hole bandstructure in nanowires.

Problem:

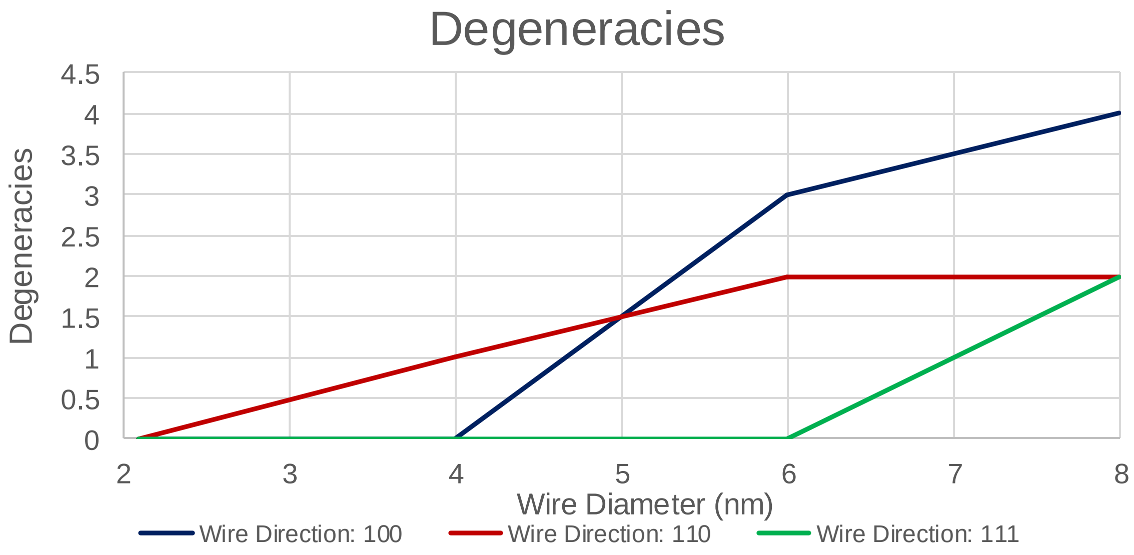
- Which wire direction is recommended at a diameter of 2.1mm?

Results / Impact:

- There are degeneracies at diameters >2.1nm.
- The best wire direction for a 2.1nm diameter wire is in the 100 direction, due to the decreased mass.

Approach:

- A silicon nanowire was modeled in NanoHub's BandstructureLab tool, varying the wire diameter from 2.1nm, 4nm, 6nm, and 8nm.
- Please see NanoHub Inputs (located in the Appendix) for the inputs used in this simulation.



What We Learned

- Short Channel effects occur when Channel length is comparable to Source/Drain depletion width
  - More pronounced in Planar MOSFETs
  - Hampers device performance with scaling

- Nanowires with Gate-all-around structure restore device performance with Excellent Electrostatic Gate control over the channel.

- On/Off Current ratio, Subthreshold Swing, Effect of strain across various Gate lengths and Nanowire Diameters along with other conditions studied, and Id-Vg characteristics investigated to model Nanowire Transistors

To Conclude

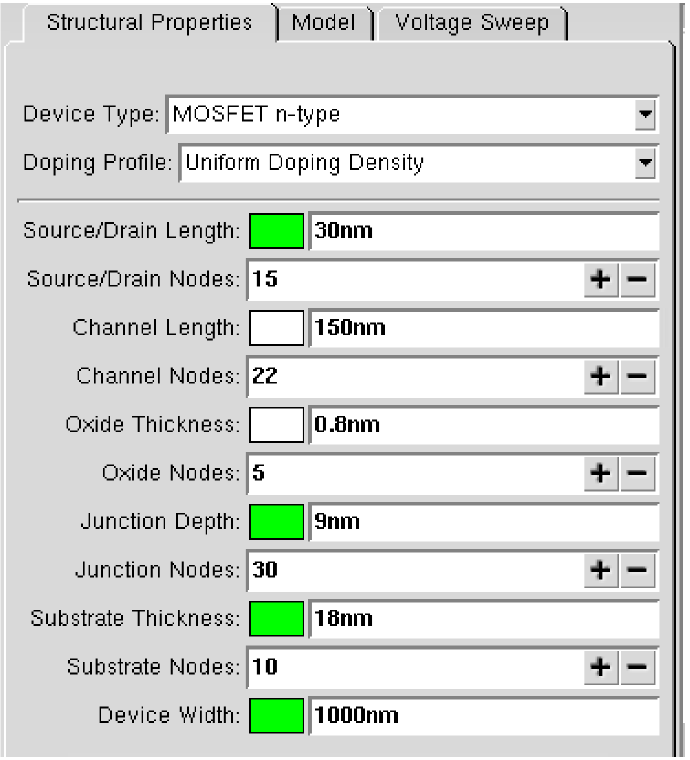
- Transistors number in the billions in individual devices that we use everyday
- You likely care about how powerful your phone is and how long its battery lasts!
- Nanowire transistors allow us to create more ideal devices for lower power and better performance
- Utilizing the design levers discussed here allows us to design the best application-specific transistors possible
- We've shown here how Nanowires outperform Planar Transistors in
  - Leakage Currents
  - On/Off Current Ratio
  - Subthreshold Swing
  - Drain-Induced-Barrier-Lowering
- Nanowire scale allows their density to continue increasing
- Nanowires look to usher in a new era of performance and efficiency!

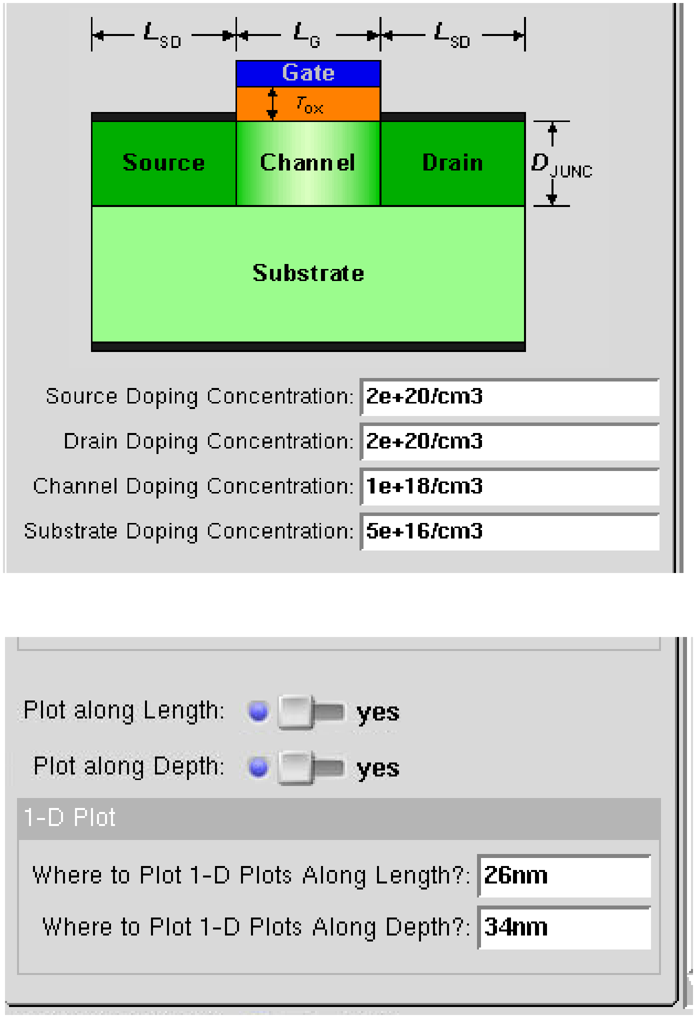
Appendices

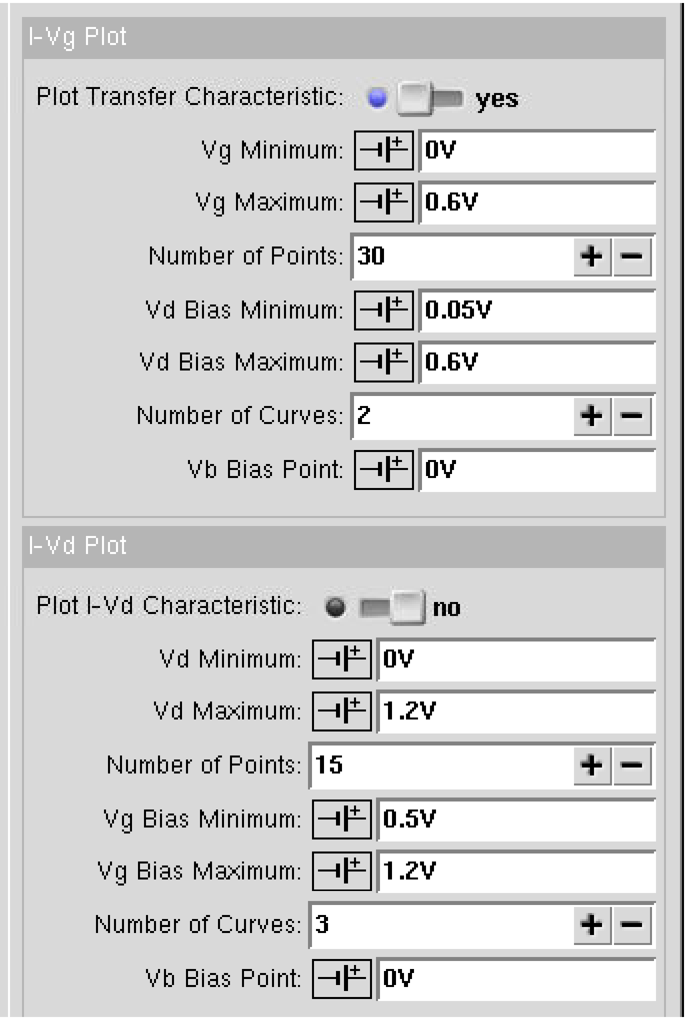
Team “Electron Highway"

- This team consisted of three members with distinct backgrounds split between academic research and industry experience.
- The team effort focused on collaboration rather than a division of labor.
- To build a basis for this project, every member attempted Challenge 1, 2, & 3 and collaborated on the final solution.
- All other challenges had at least two members, with members choosing challenges they were particularly interested in or had a background in. The team collaborated on the final solution.
- Utilized meetings to discuss final solutions and shared messing app to collaborate when "stuck" on a problem

Classical MOSFET Limitations (NanoHub MOSFET Inputs)

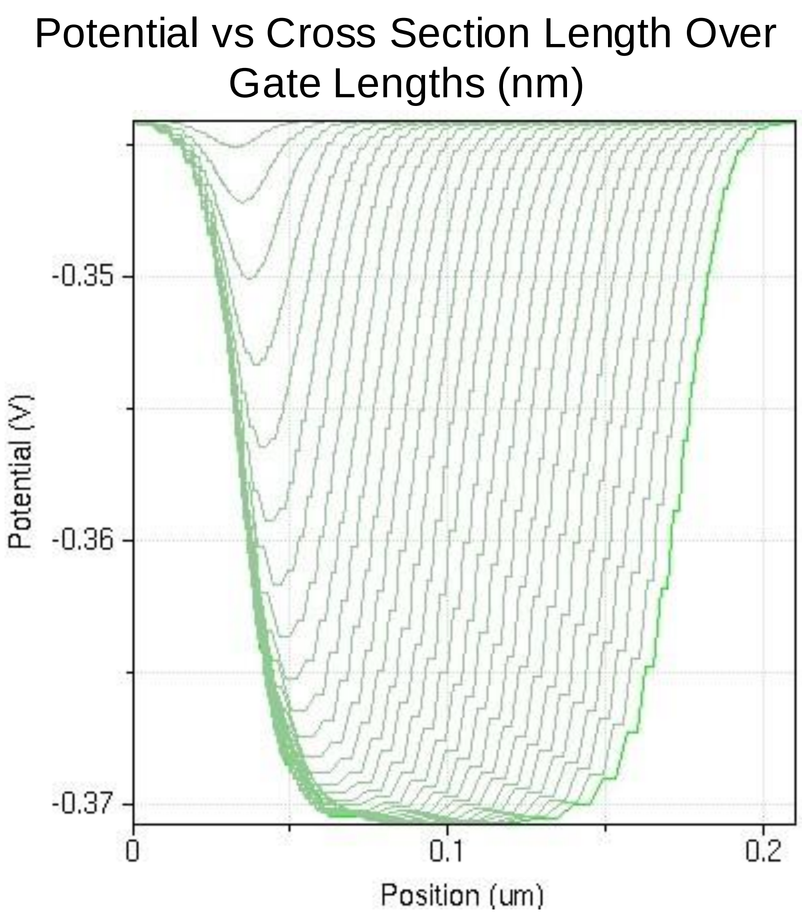


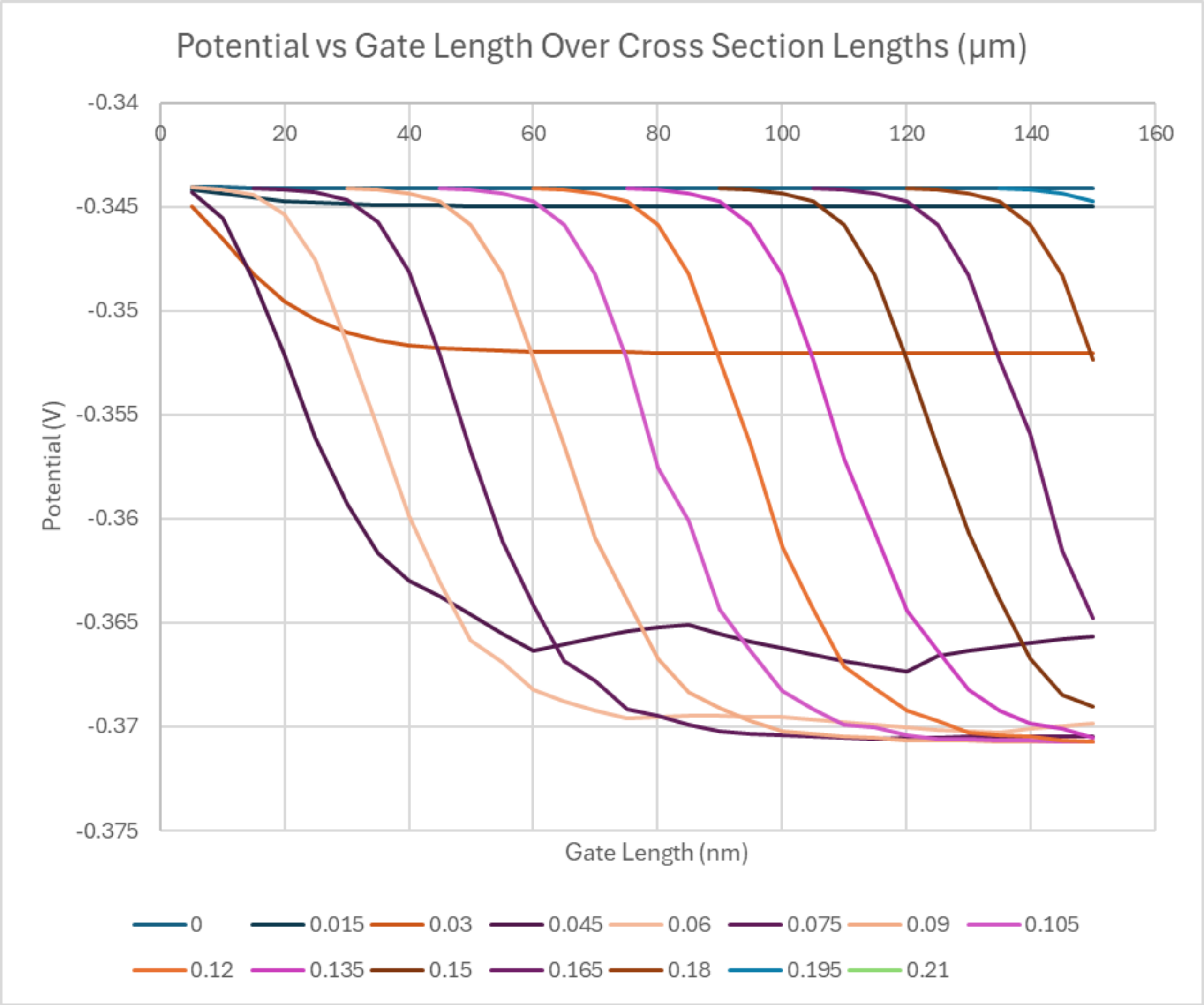




Tool located at:
https://nanohub.org/tools/mosfet

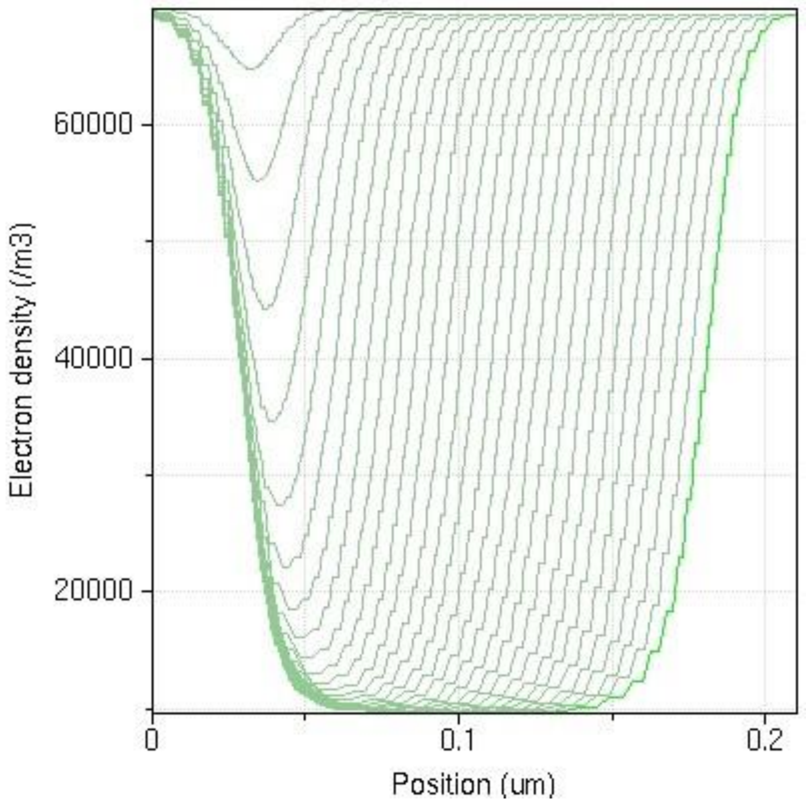
Classical MOSFET Limitations (Voltage Potentials)

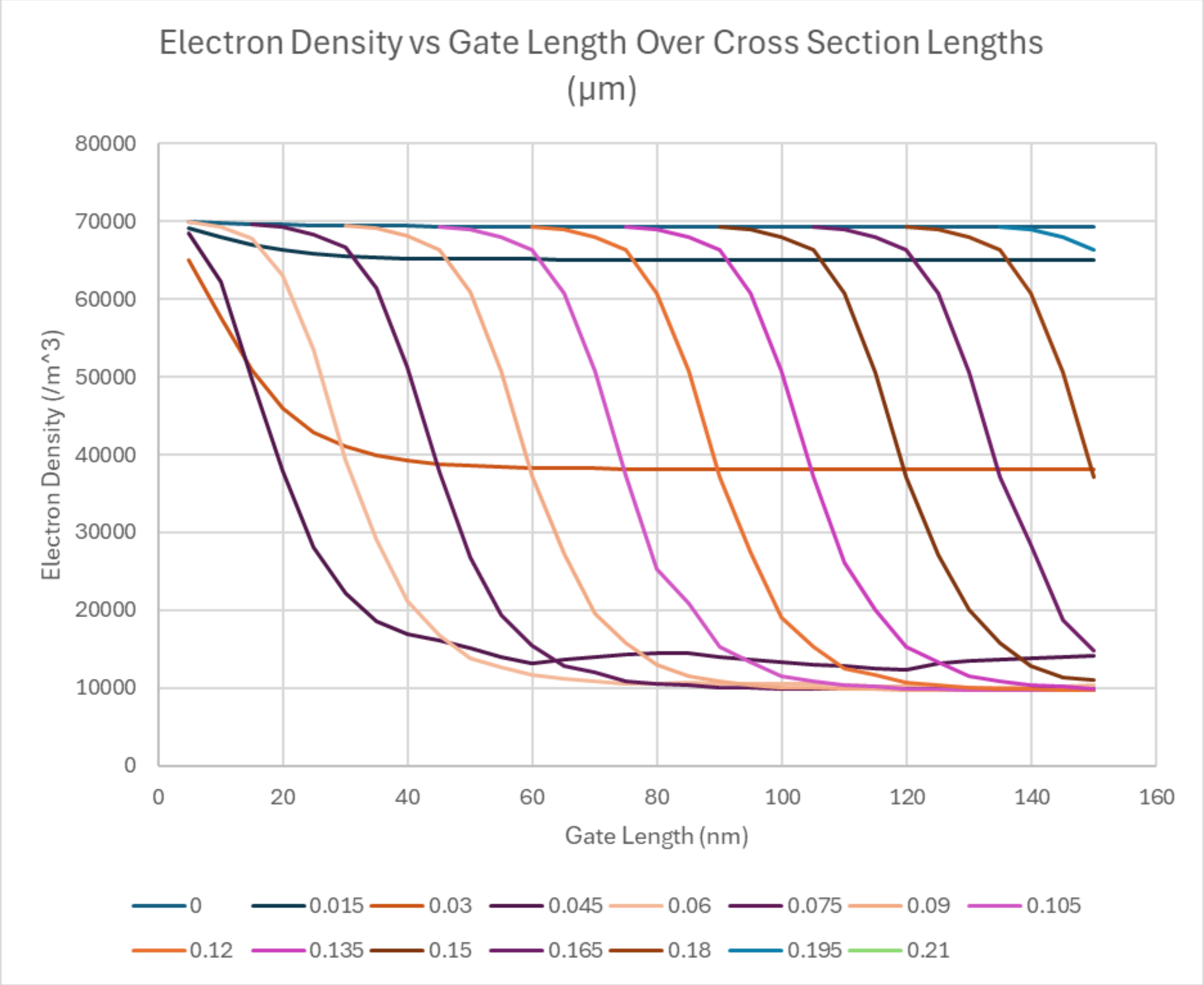




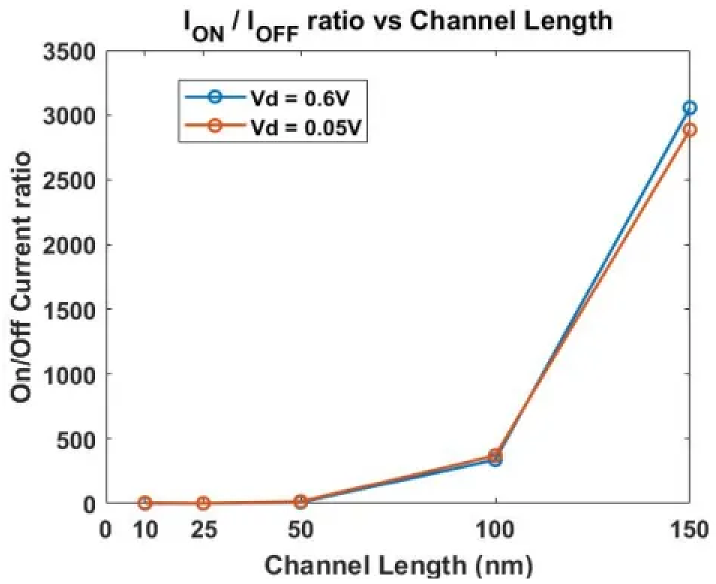
Classical MOSFET Limitations (Electron Densities)

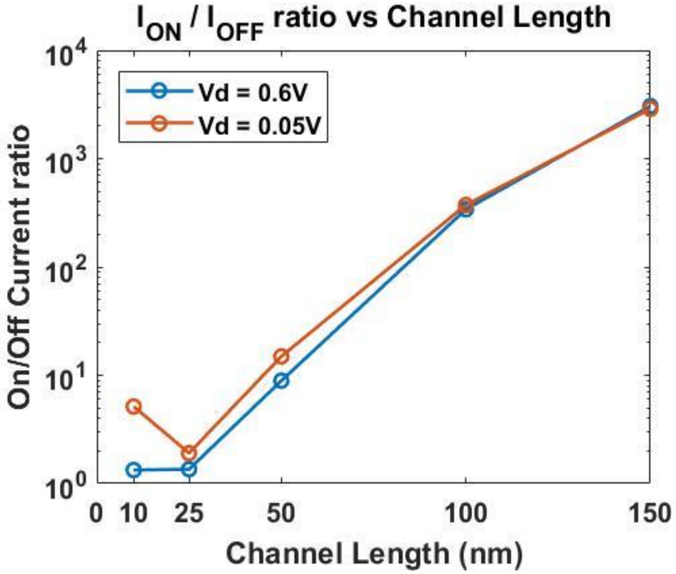
Electron Density vs Cross Section Length Over Gate Lengths (nm)

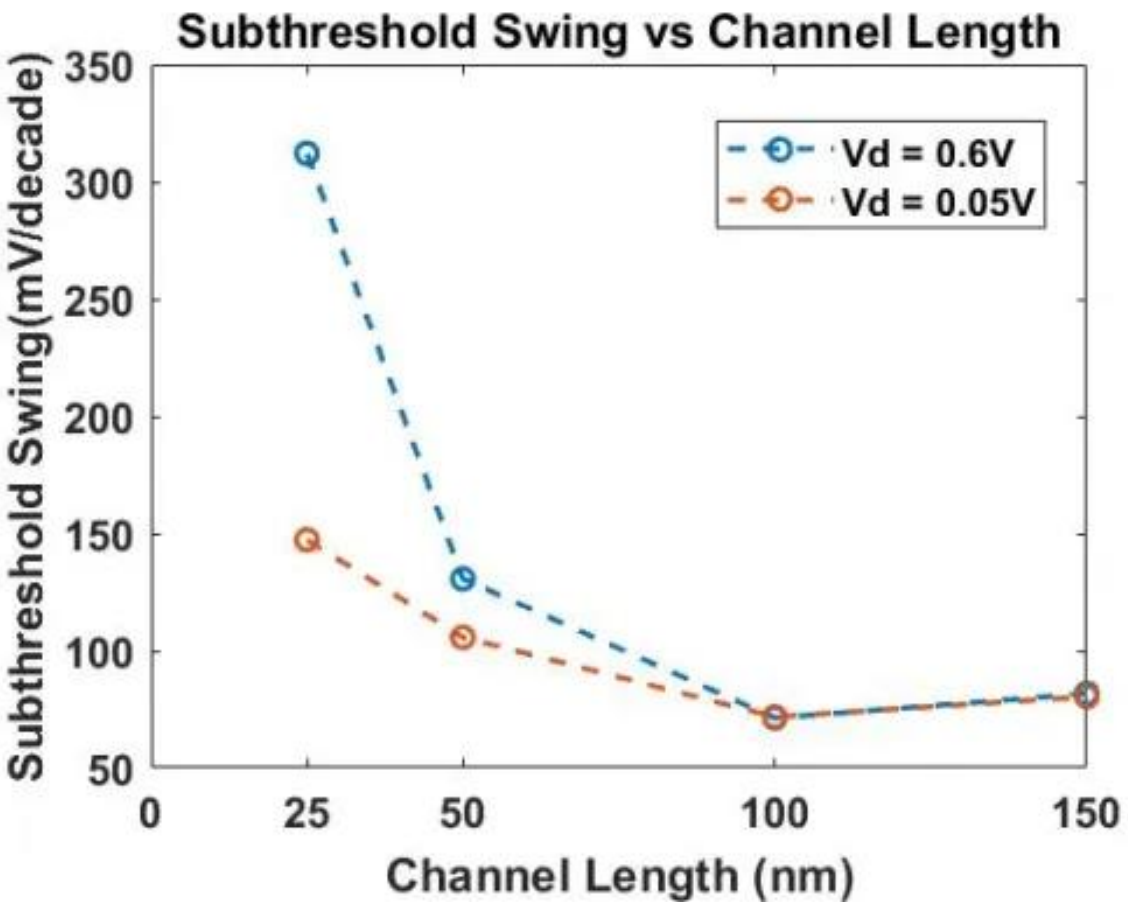




Classical MOSFET Limitations (Transistor Features)

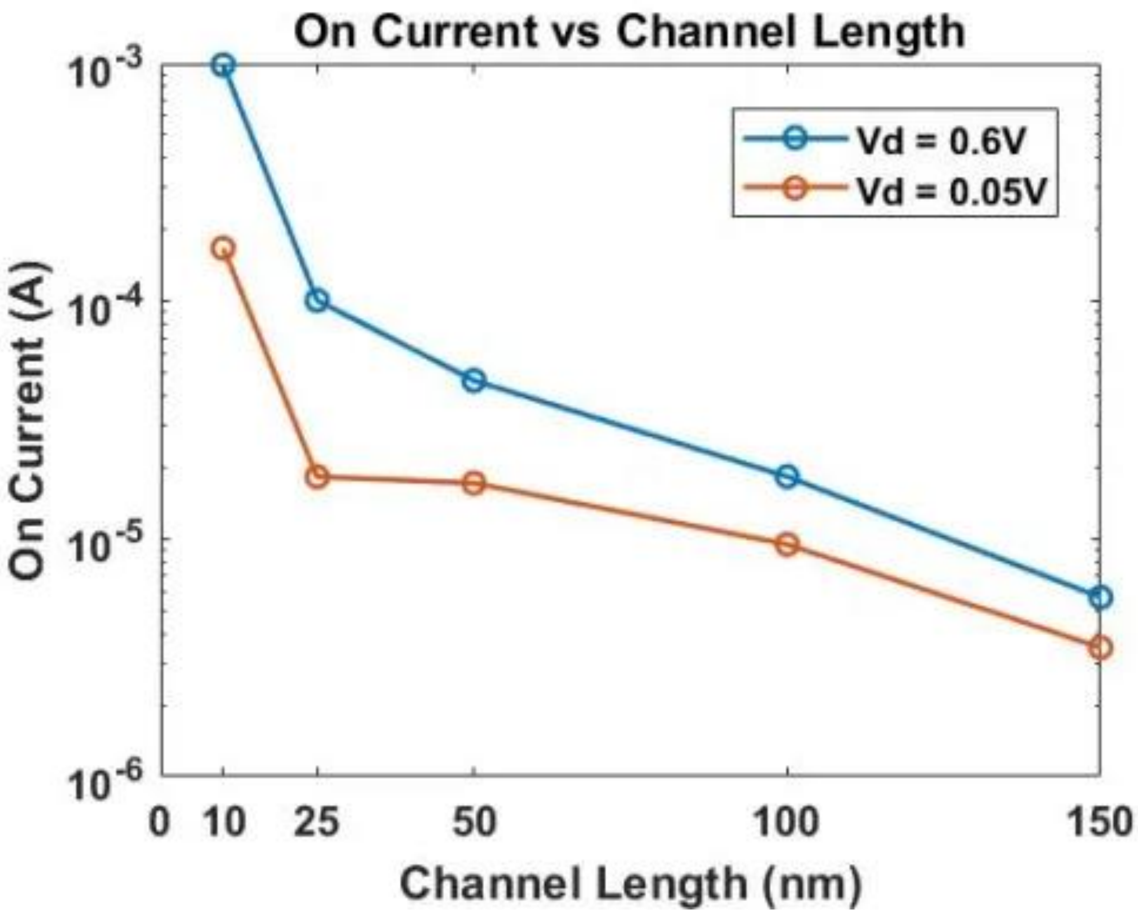


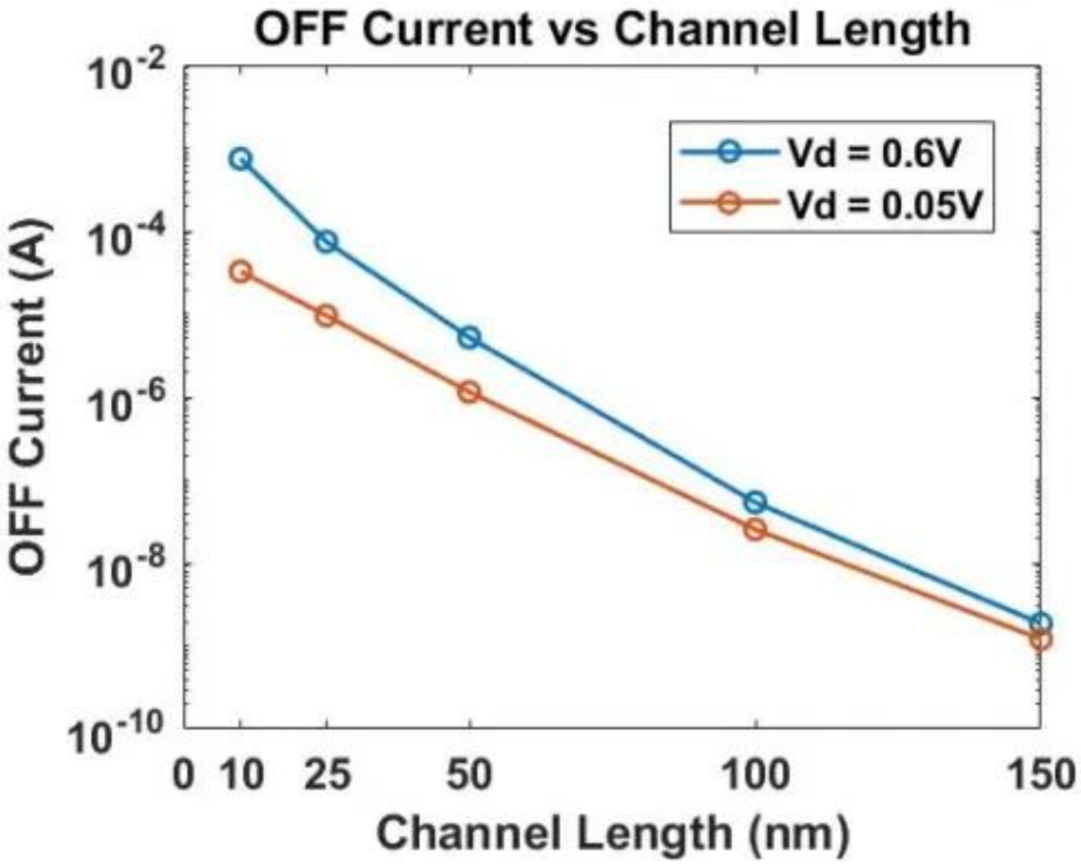




Note, due to the increasingly high leakage currents at low channel lengths, 10nm and 5nm subthreshold swing values were excluded from the above plot.

Classical MOSFET Limitations (Transistor Features)





Nanowire with Drift Diffusion (NanoHub NANOFINFET Inputs)

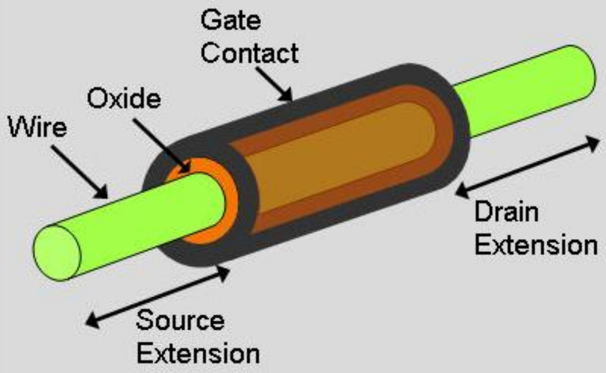
All default settings were utilized, except as where shown (red boxes mark variable inputs):

Device Type

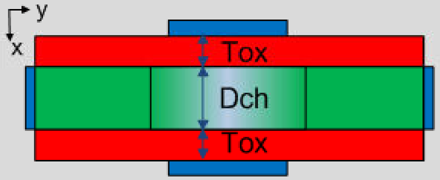
Class: Nanowire

Spec

Gate Type: Metal

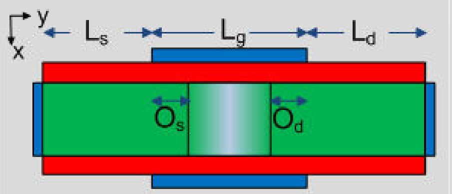


Geometry-X | Geometry-Y | Geometry-Z | Doping | Gaussian doping



Diameter - Dch:	2.1nm
Oxide thickness - Tox:	2.5nm
Channel width - Wch:	30nm
Oxide thinkness 1 - Tox1:	2.5nm
Oixde thickness 2 - Tox2:	2.5nm
Substrate - S:	100nm

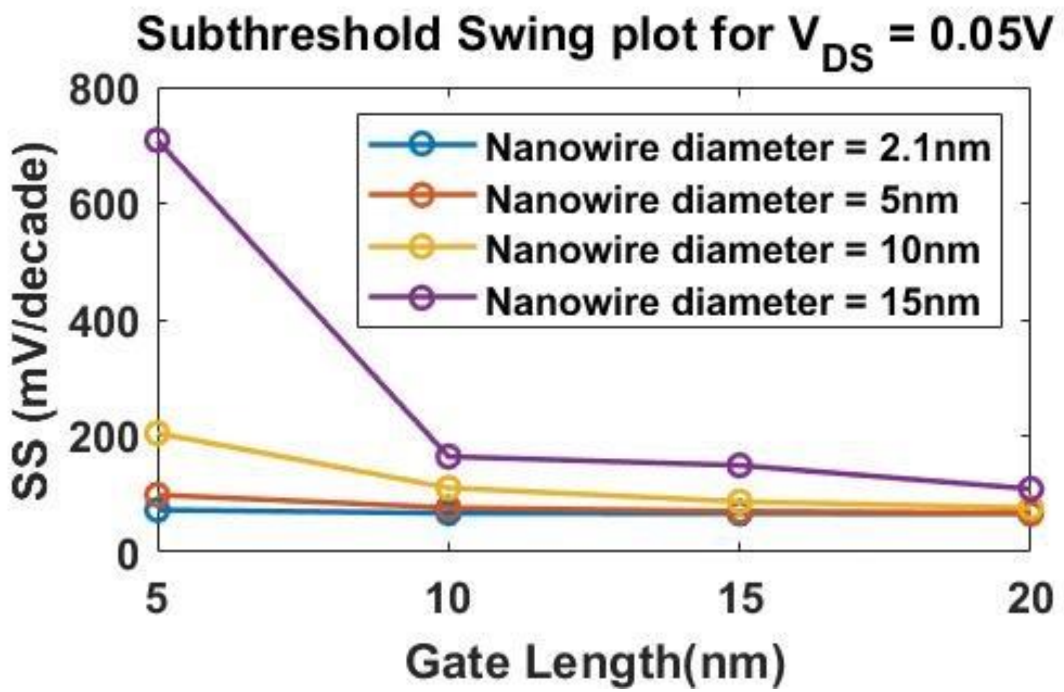
Geometry-X | Geometry-Y | Geometry-Z | Doping | Gaussian doping

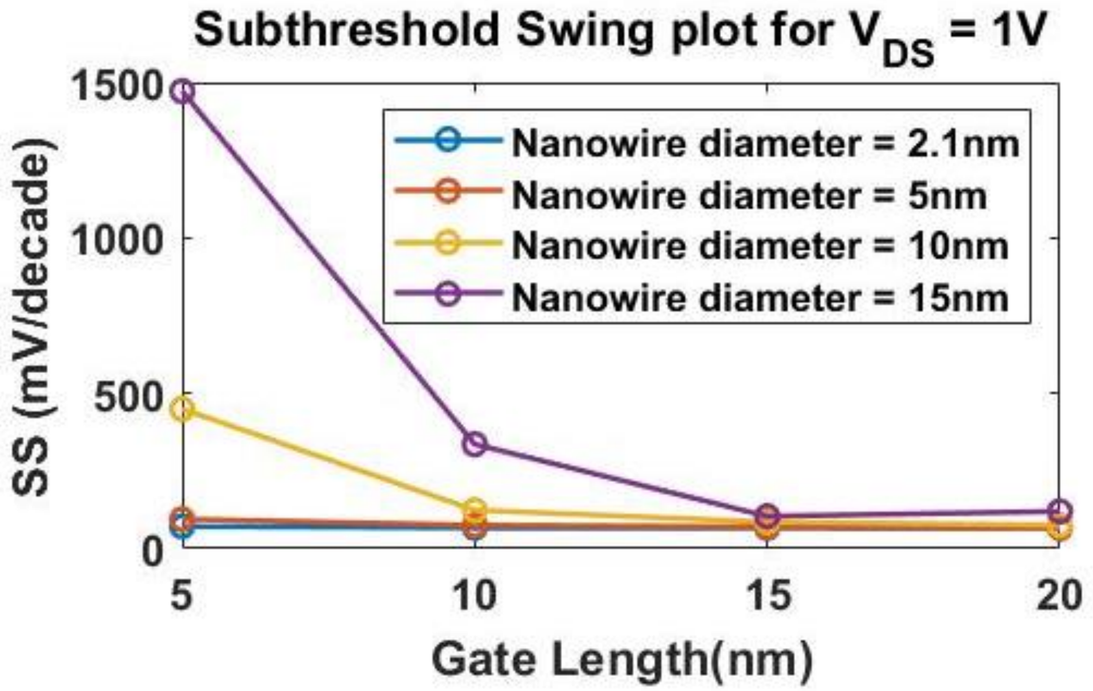


Gate length - Lg:	20nm
Source extension length - Ls:	20nm
Drain extension length - Ld:	20nm
Gate overlap to source - Os:	2nm
Gate overlap to drain - Od:	2nm
Spacer:	15nm

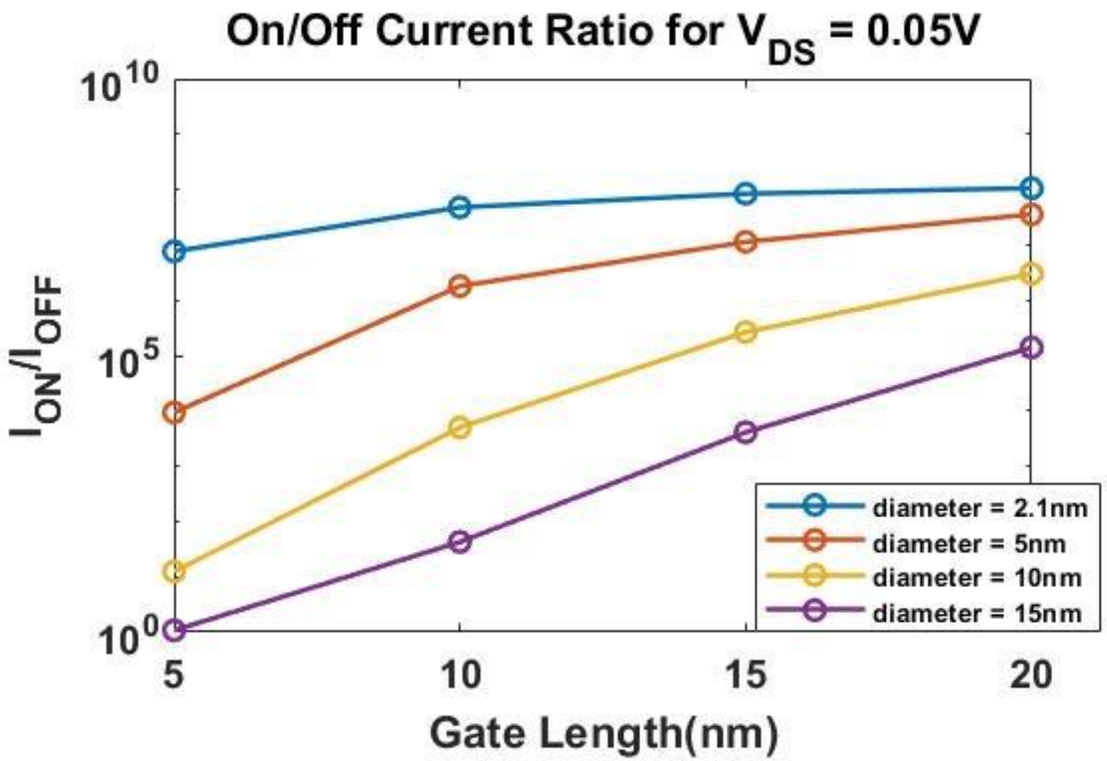
Tool located at:
https://nanohub.org/tools/nanofinfet

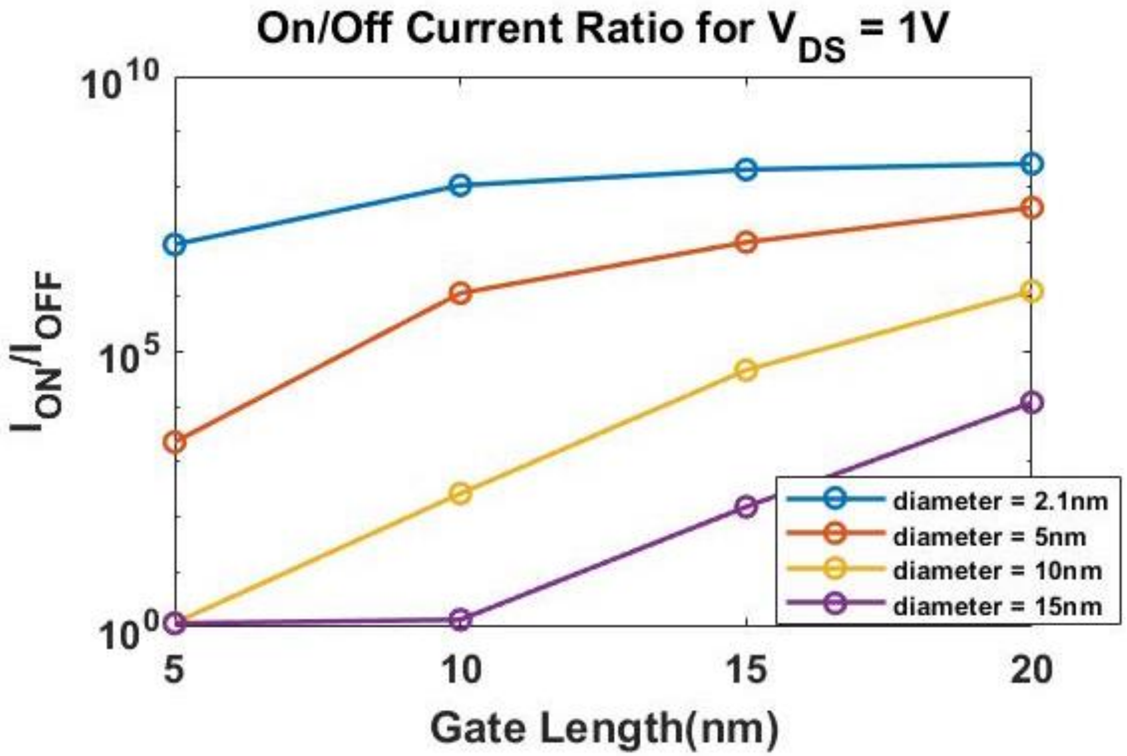
Nanowire with Drift Diffusion (Subthreshold Swing)



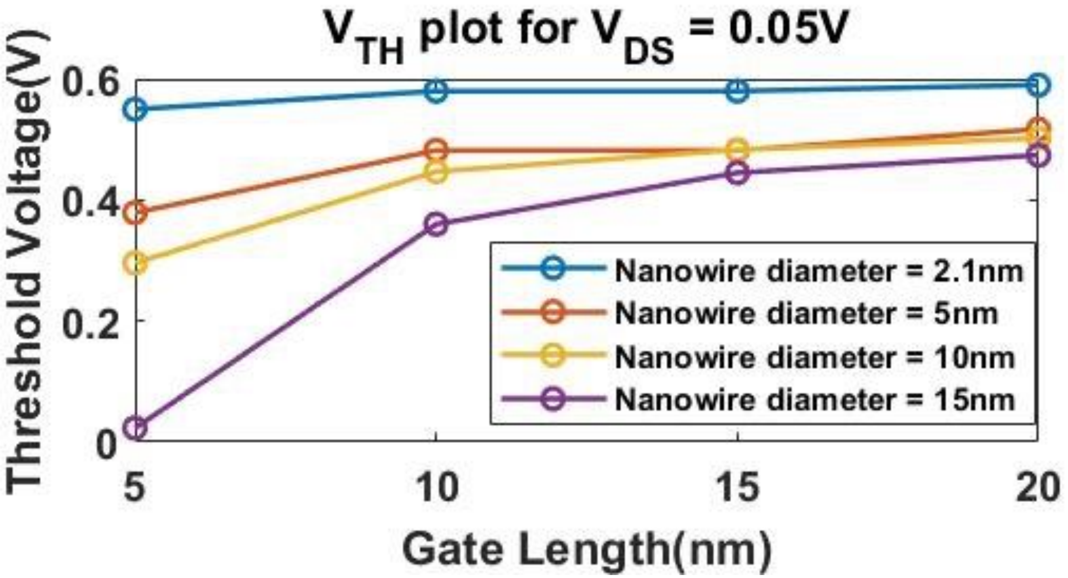


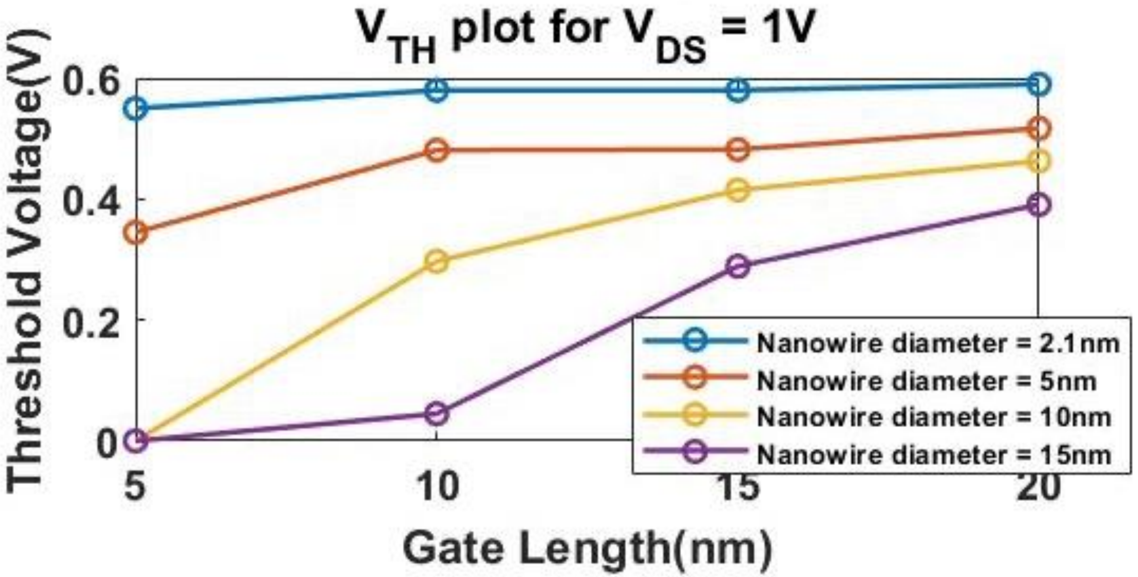
Nanowire with Drift Diffusion (On/Off Current Ratio)



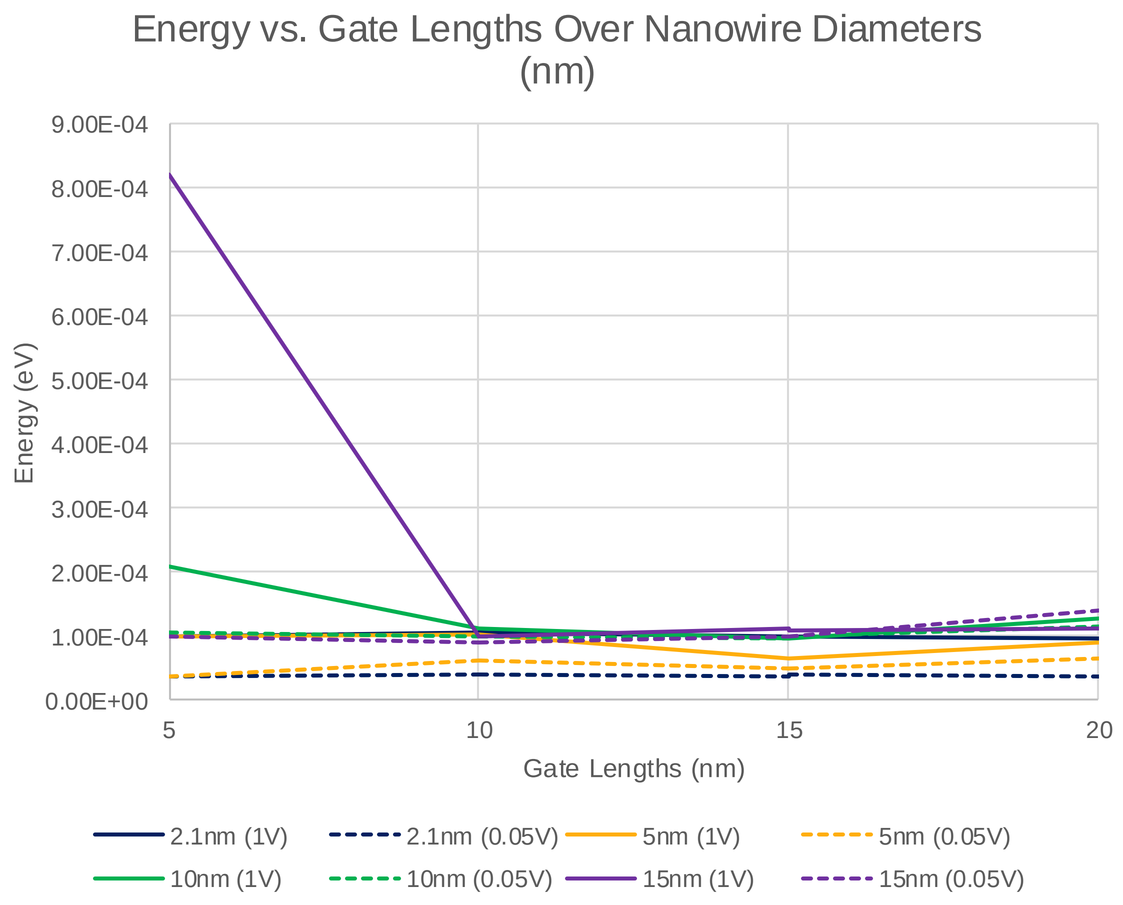


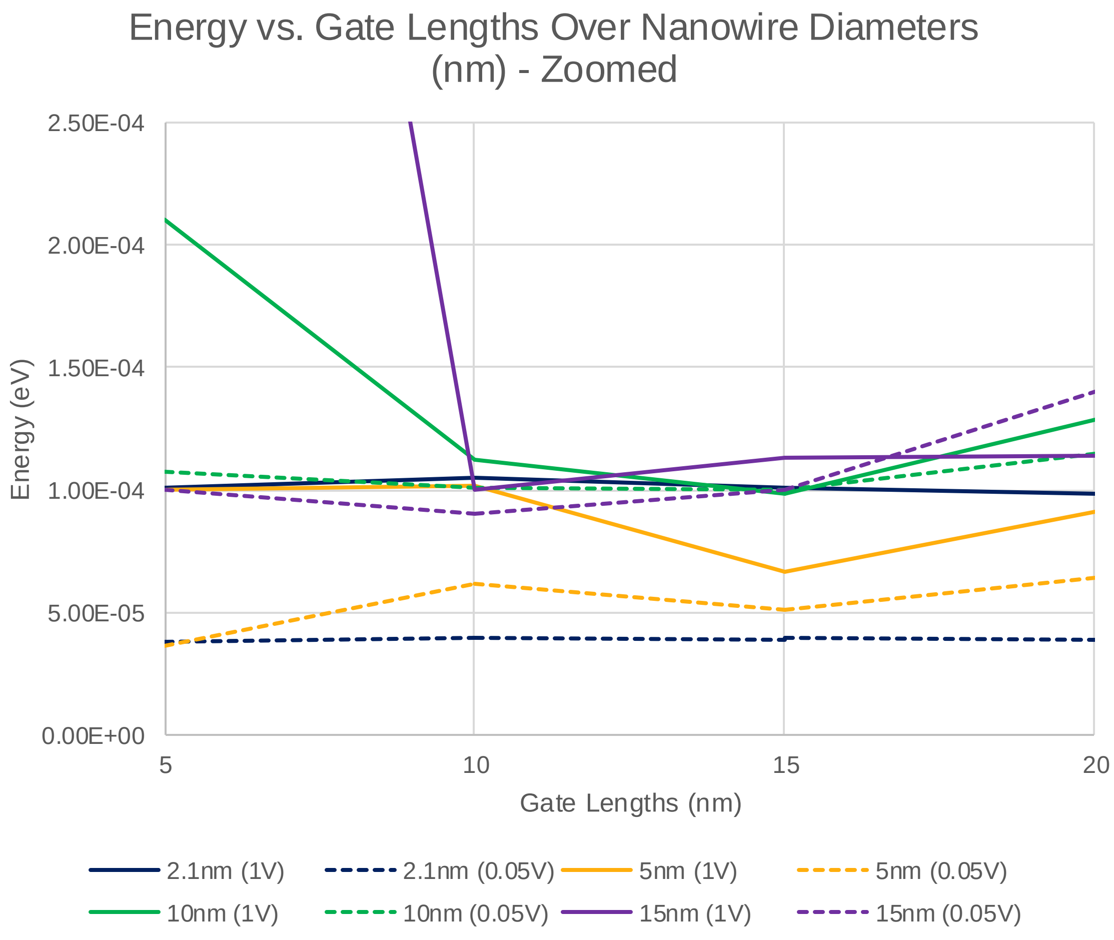
Nanowire with Drift Diffusion (Threshold Voltage)



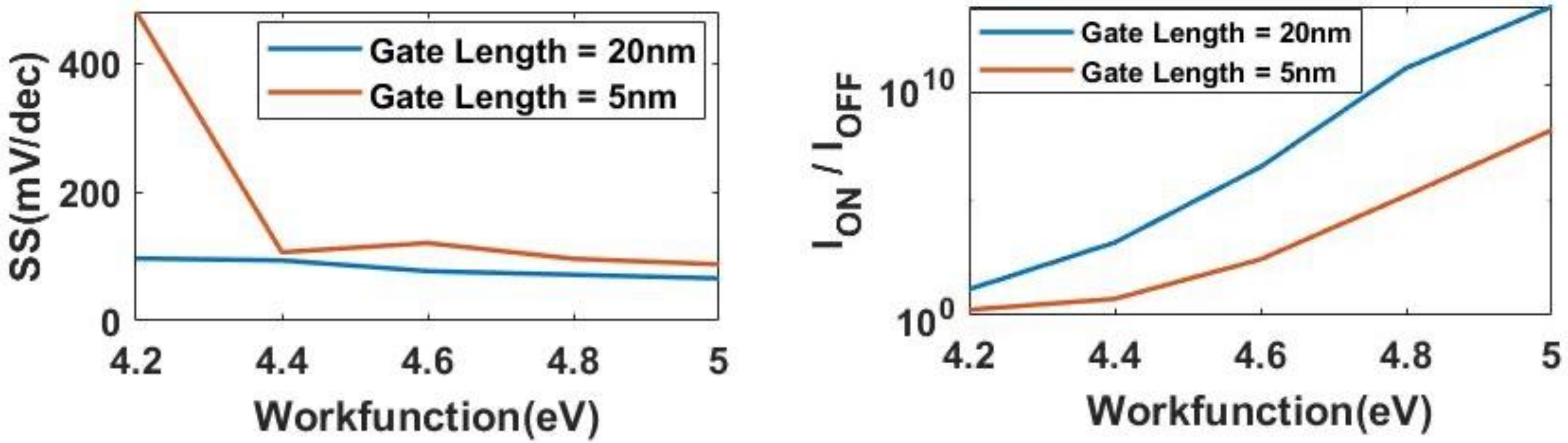


Nanowire with Drift Diffusion (Energy)

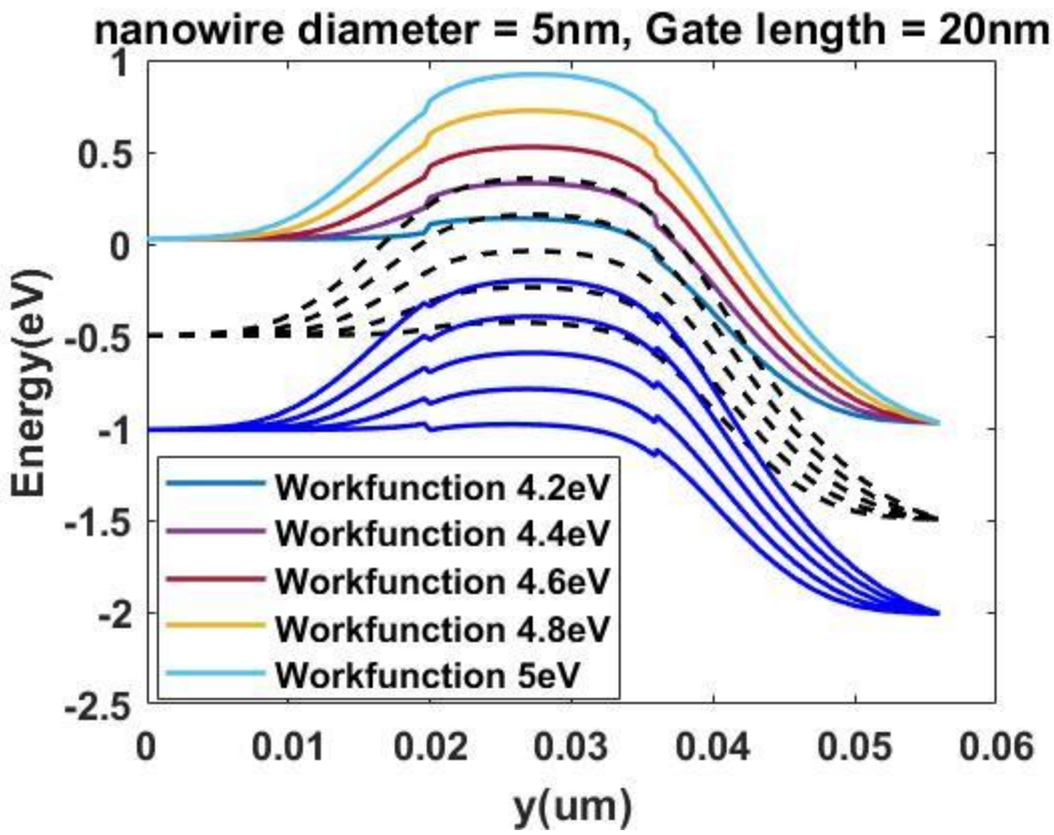


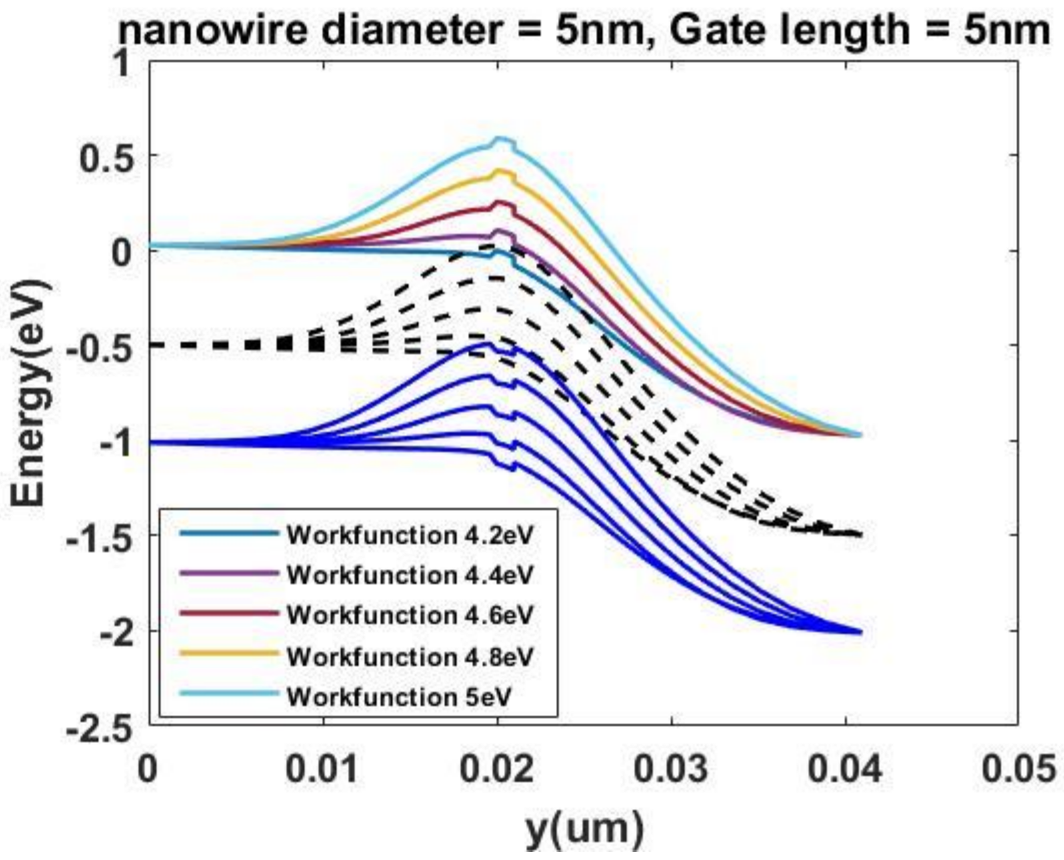


Nanowire with Drift Diffusion – Workfunction Variations and Gate Potential Analysis (Transistor Parameters)

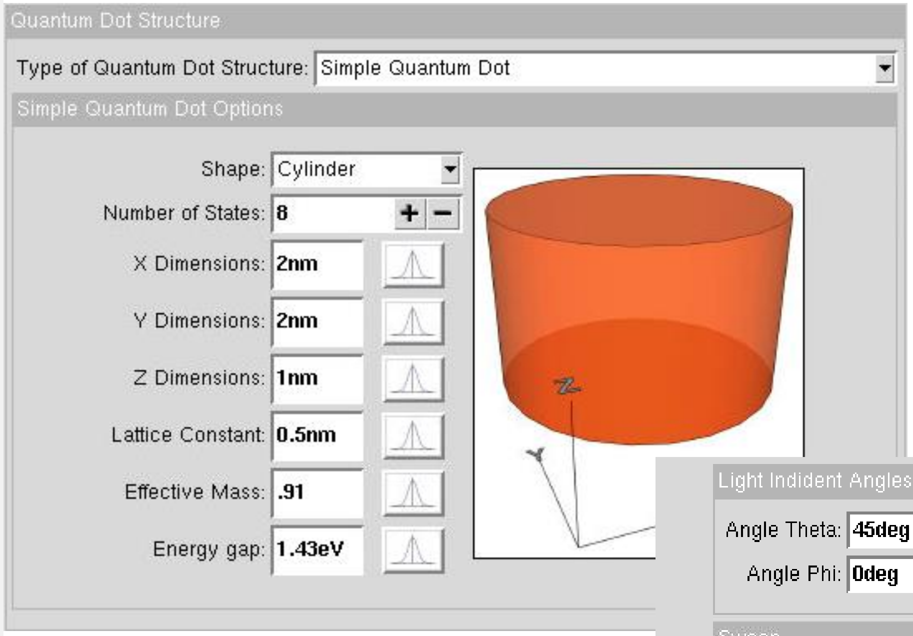


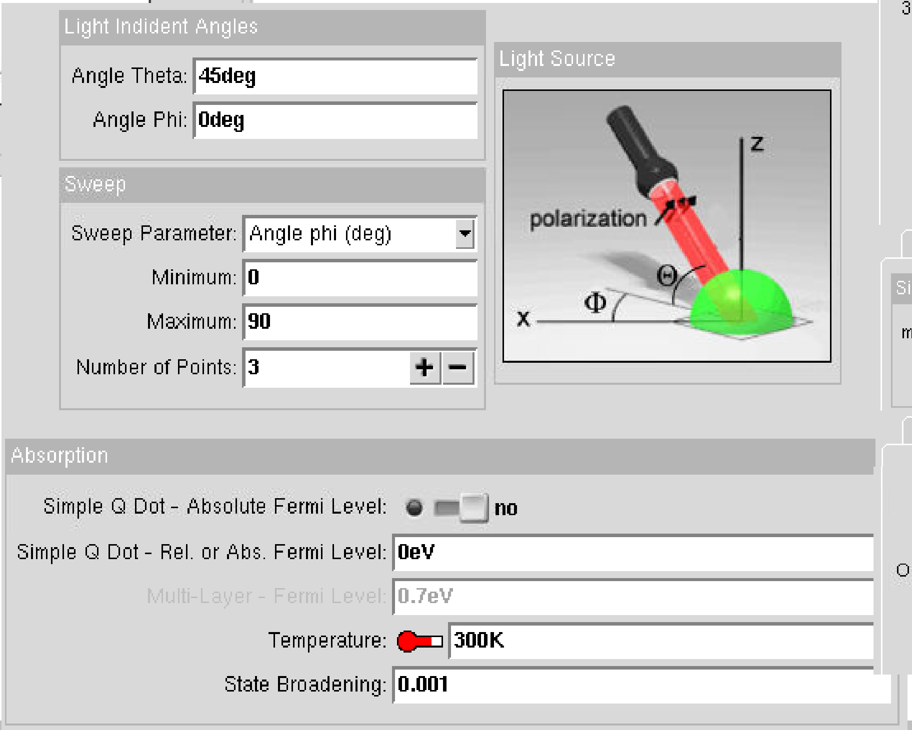
Nanowire with Drift Diffusion – Workfunction Variations and Gate Potential Analysis (Energy)

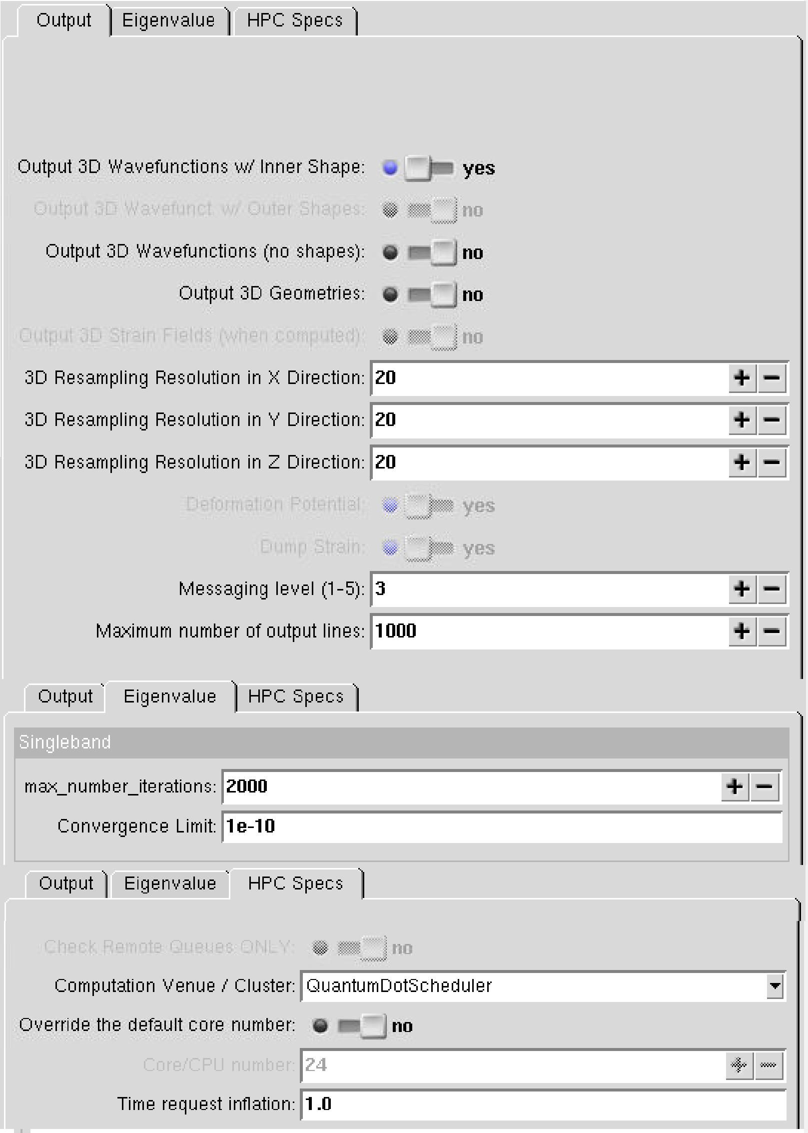




Nanowire Modes and Gating (NanoHub Quantum Dot Lab Inputs)



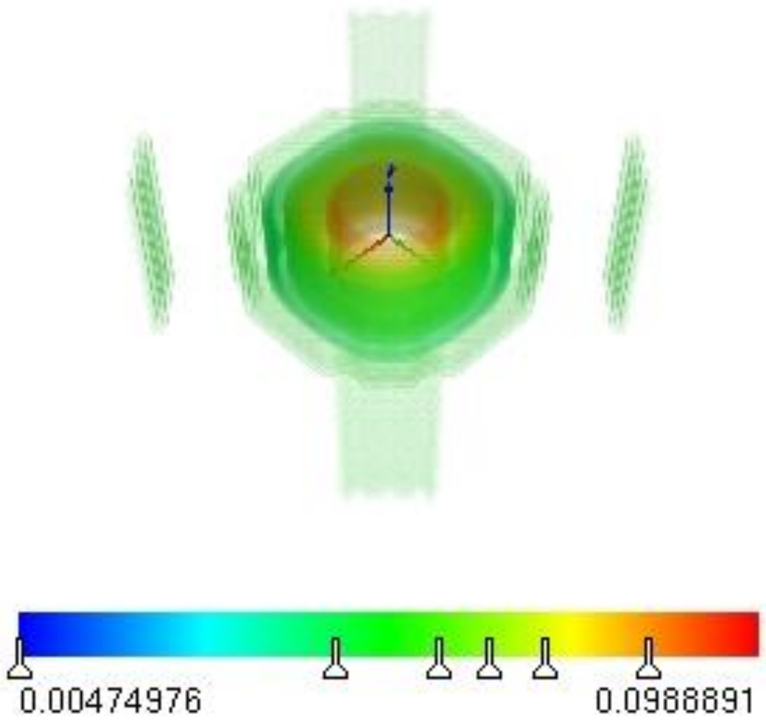




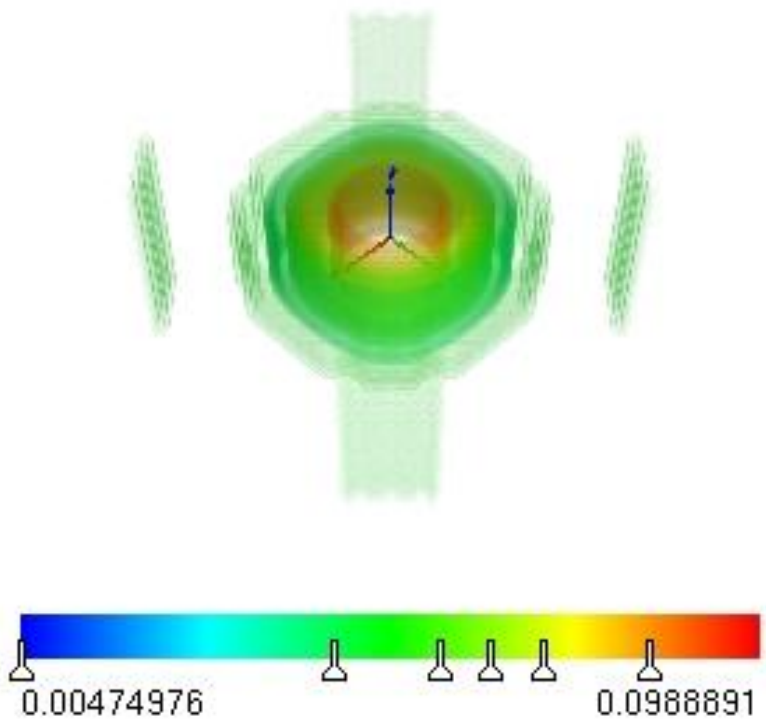
Tool located at: https://nanohub.org/tools/qdot

Nanowire Modes and Gating (Wavefunctions)

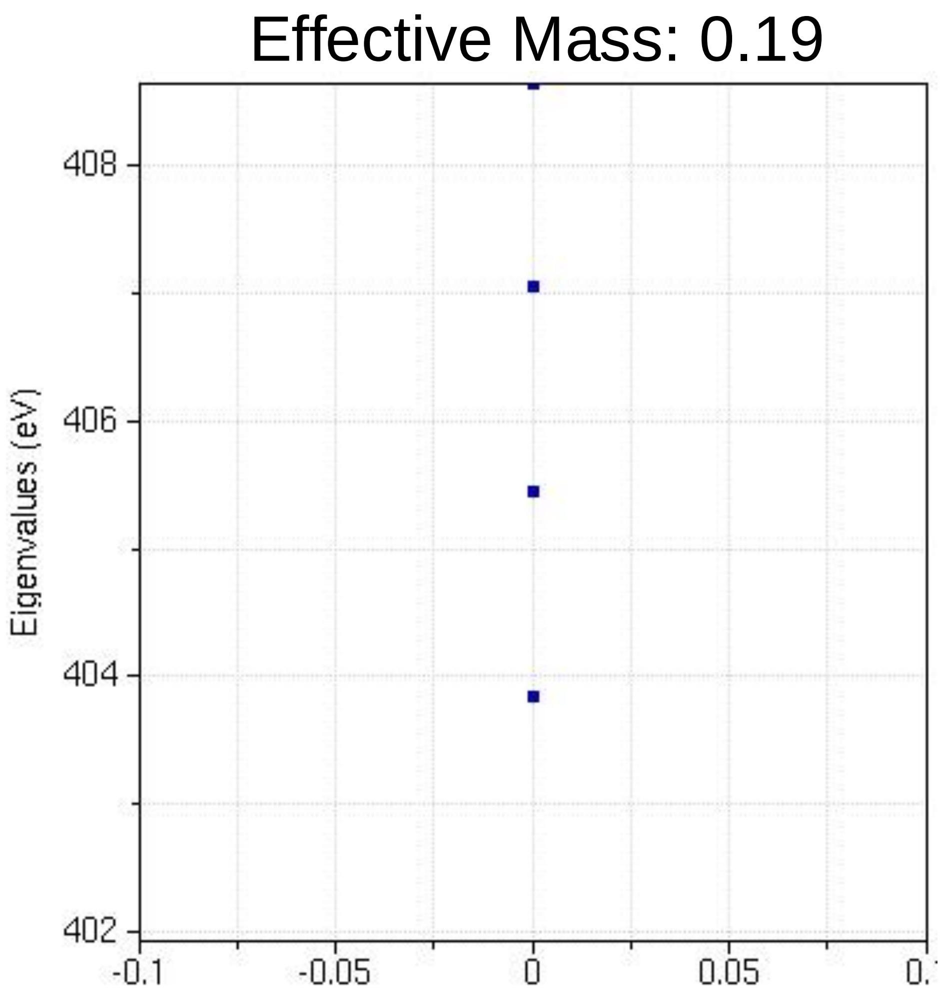
Effective Mass: 0.19

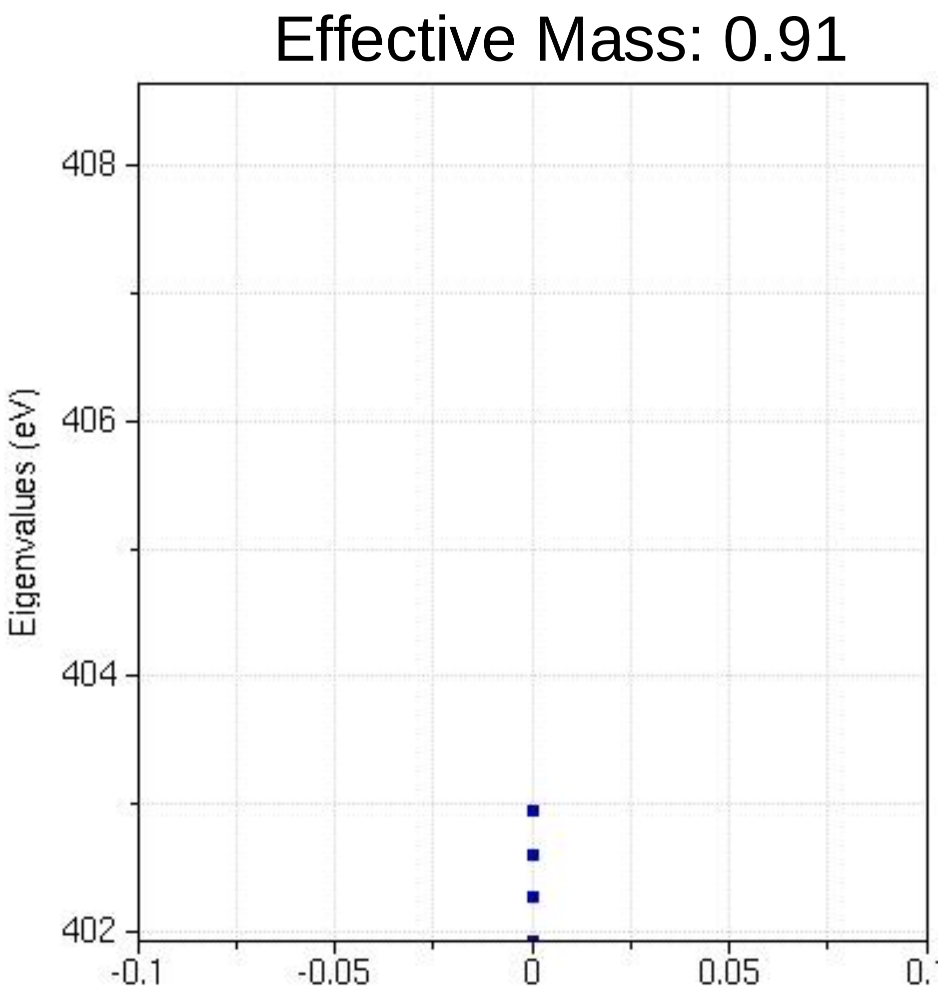


Effective Mass: 0.91

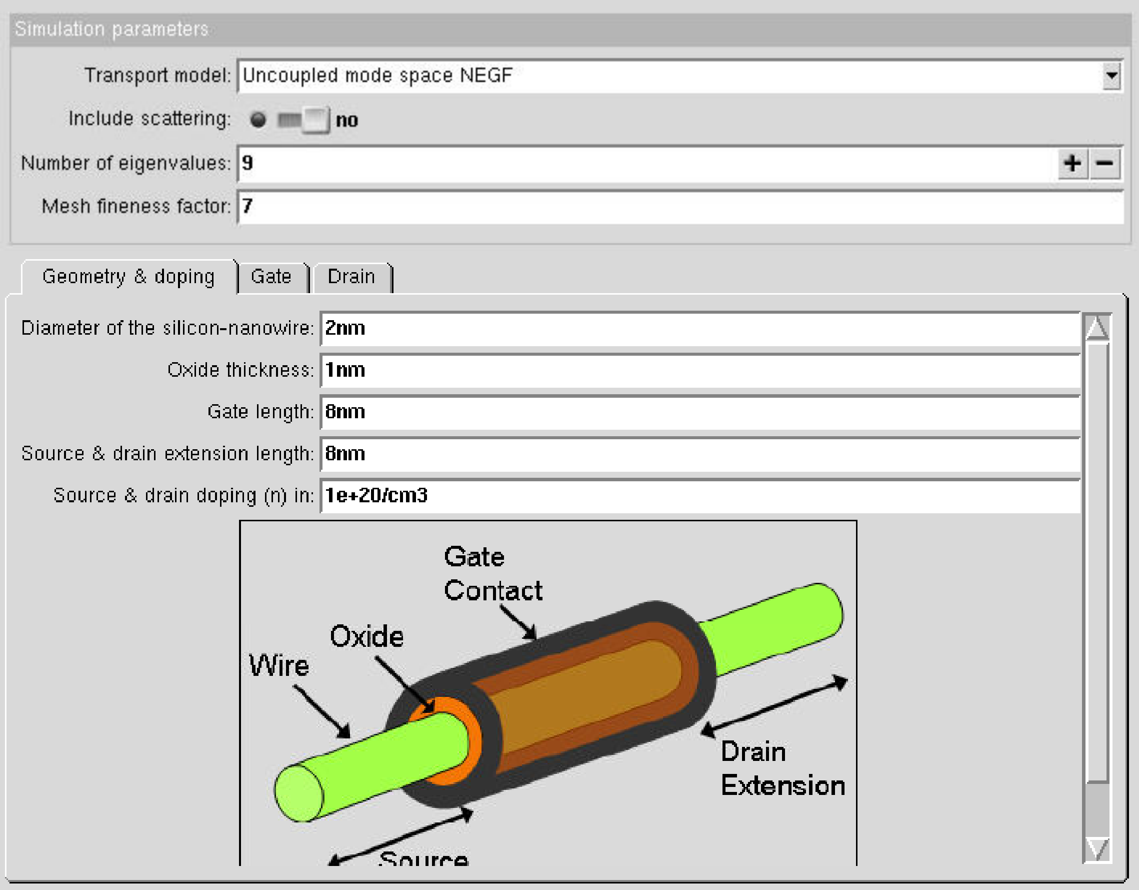


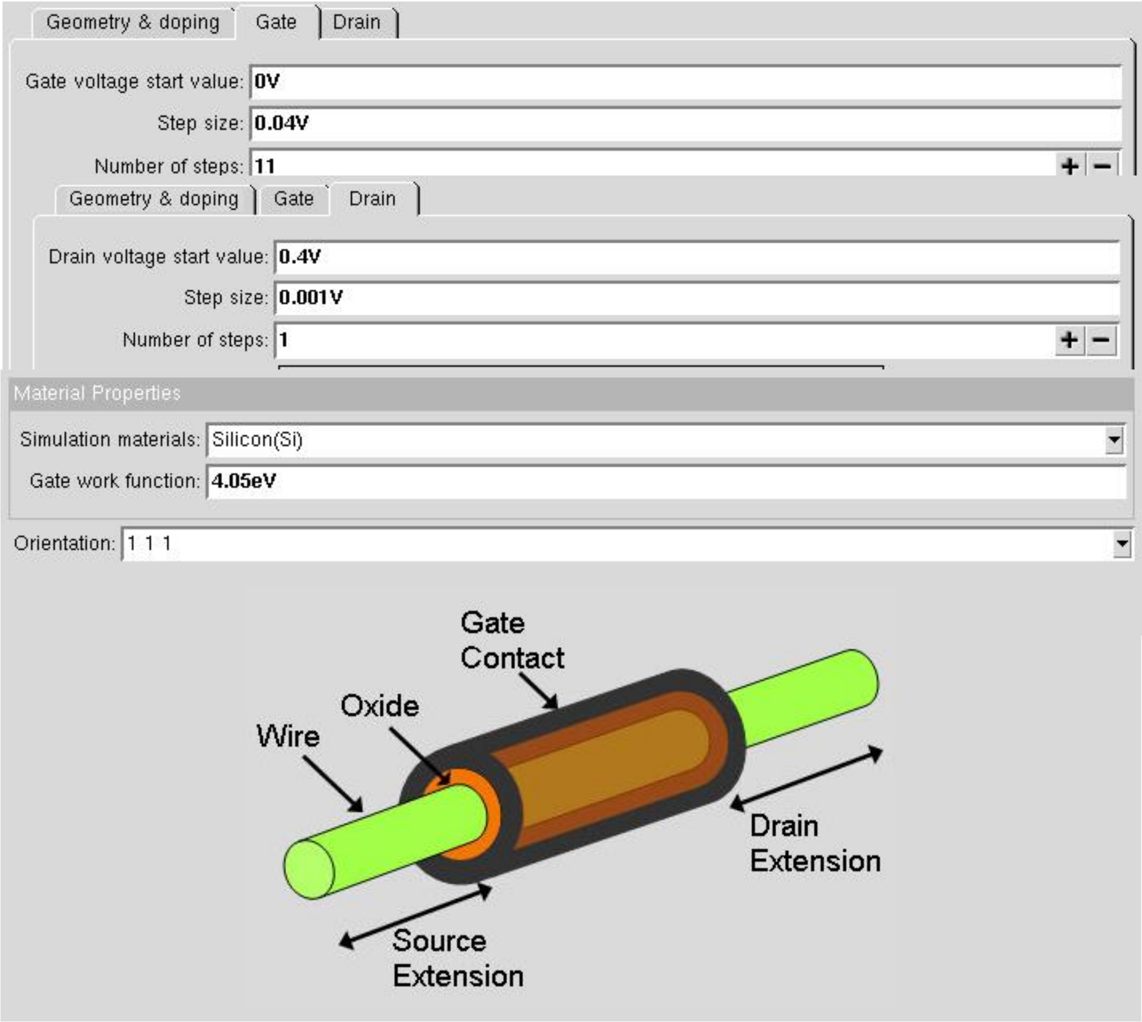
Nanowire Modes and Gating (Eigen Energies)





Nanowire Modes and Gating (NanoHub Nanowire Inputs)

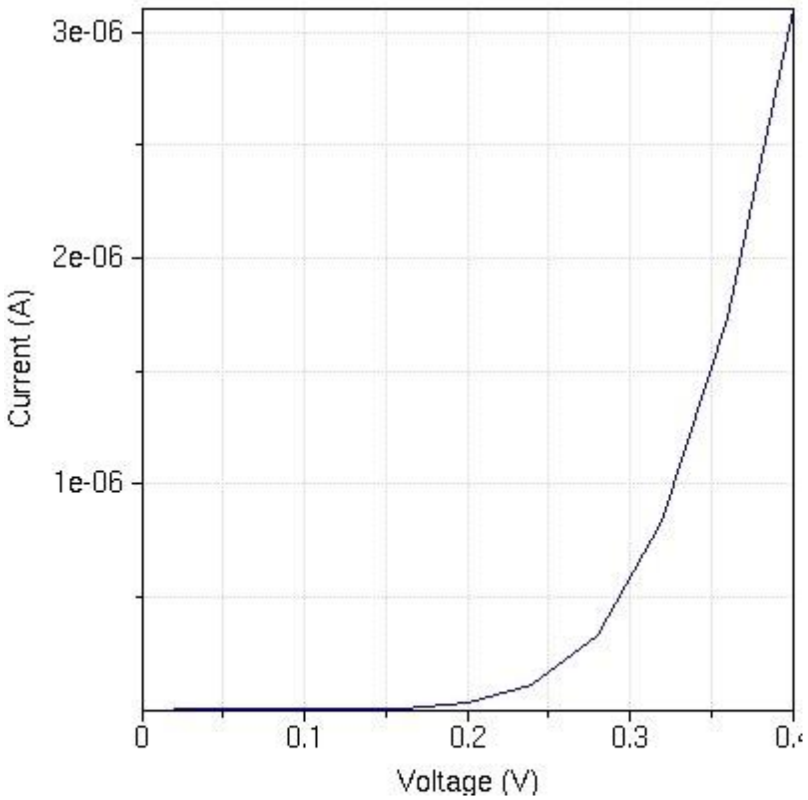




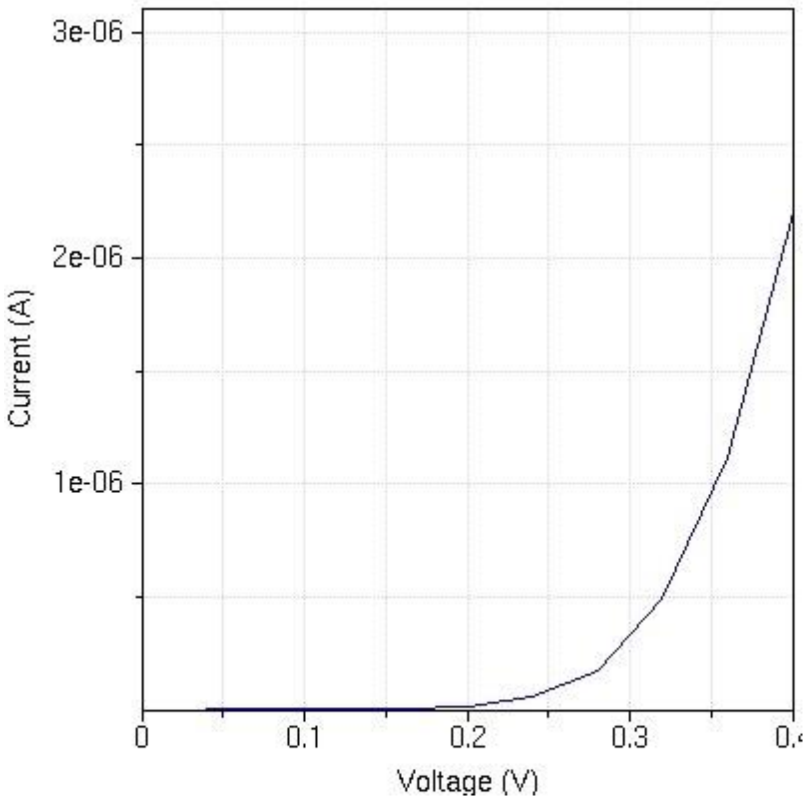
Tool located at:
https://nanohub.org/tools/nanowire

Nanowire Modes and Gating (I-Vg Curves)

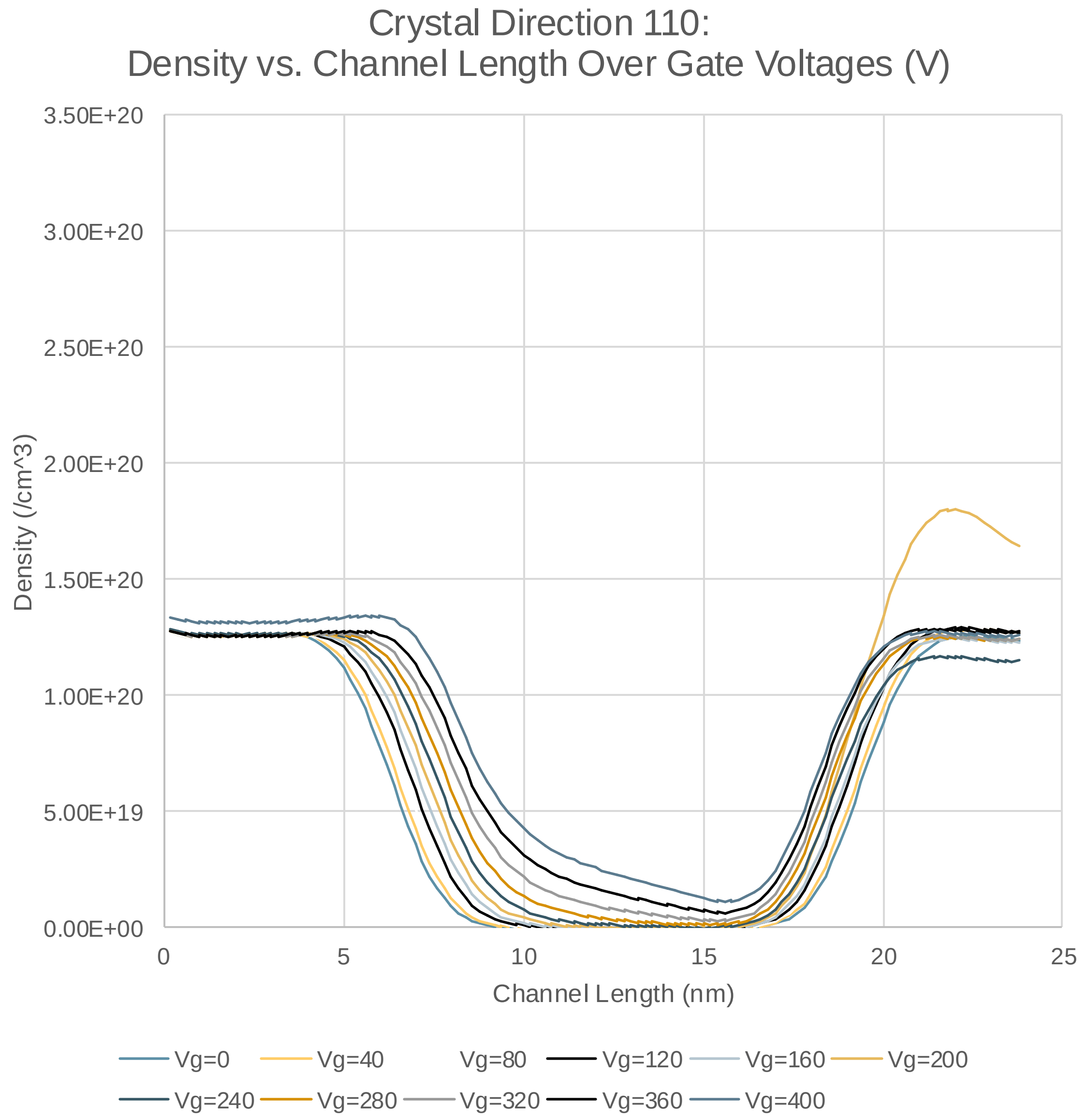
Crystal Direction: 110

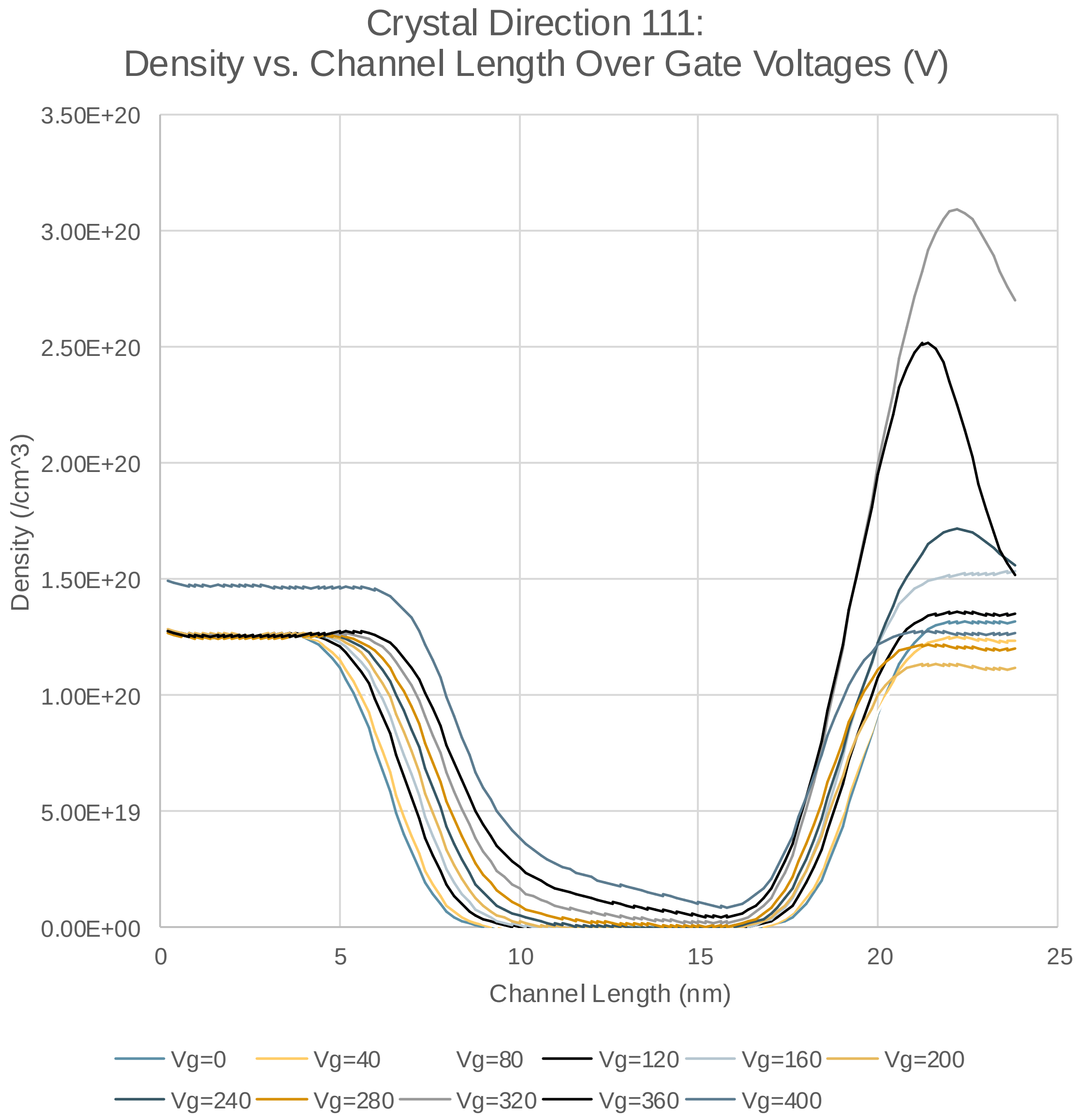


Crystal Direction: 111



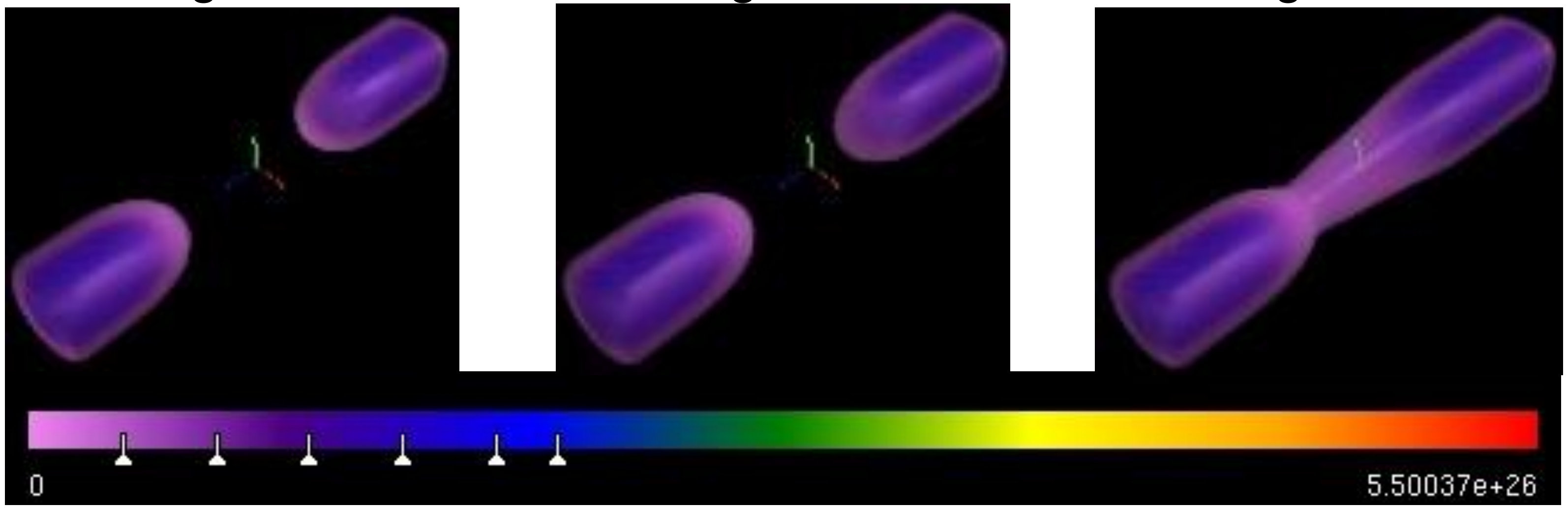
Nanowire Modes and Gating (1D Electron Densities)





Nanowire Modes and Gating (3D Electron Densities)

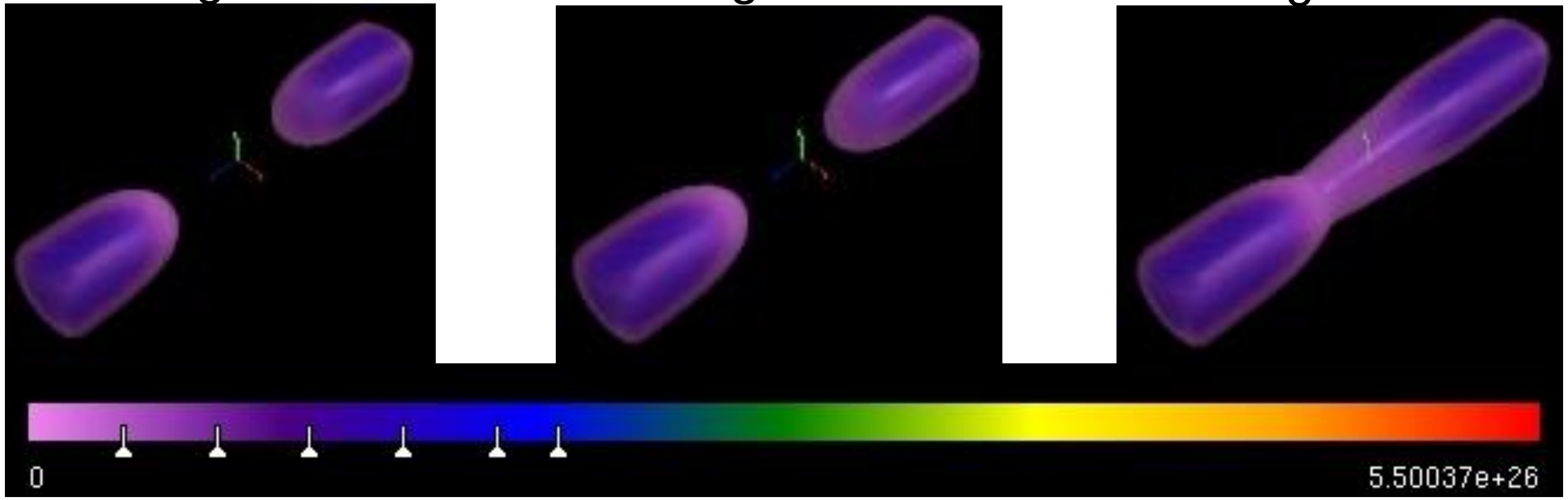
Vg=0 Vg=200 Vg=400



Crystal Direction: 110

Crystal Direction: 111

Vg=0 Vg=200 Vg=400



Nanowire Realistic Bandstructure (Inputs)

All default settings were utilized, except as where shown (red boxes mark variable inputs):

1 Device Type → 2 Physics → 3 K-Space → 4 Numerics → 5 Simulate

Geometry: Nanowire (1D-periodic)

Calculation For: Electrons

Material: Si

Alloy Model: Virtual Crystal Approximation

Molar fraction: 0.5

Job Type: Calculate the wire band structure

Device cross section: Circle

Diameter: **2.1nm**

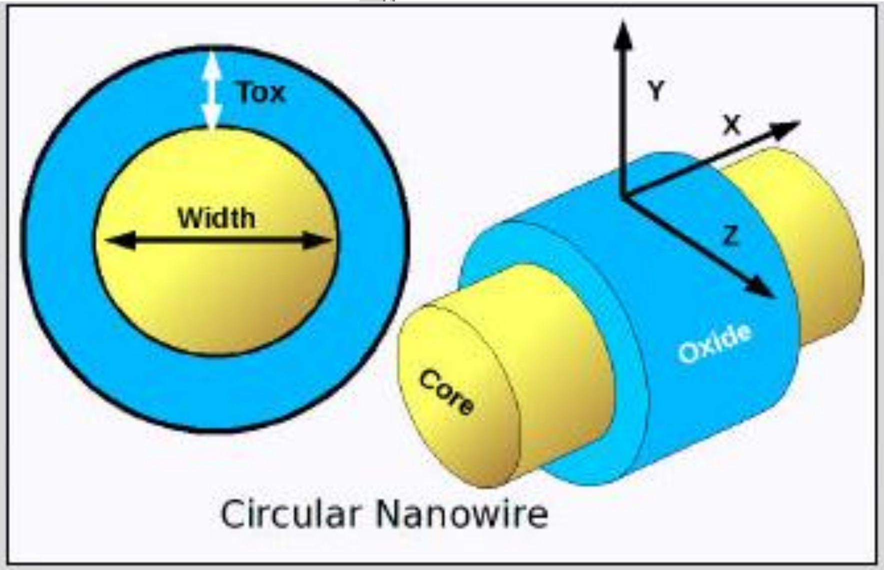
Oxide Thickness(Tox): 2.2nm

Crystal Orientation

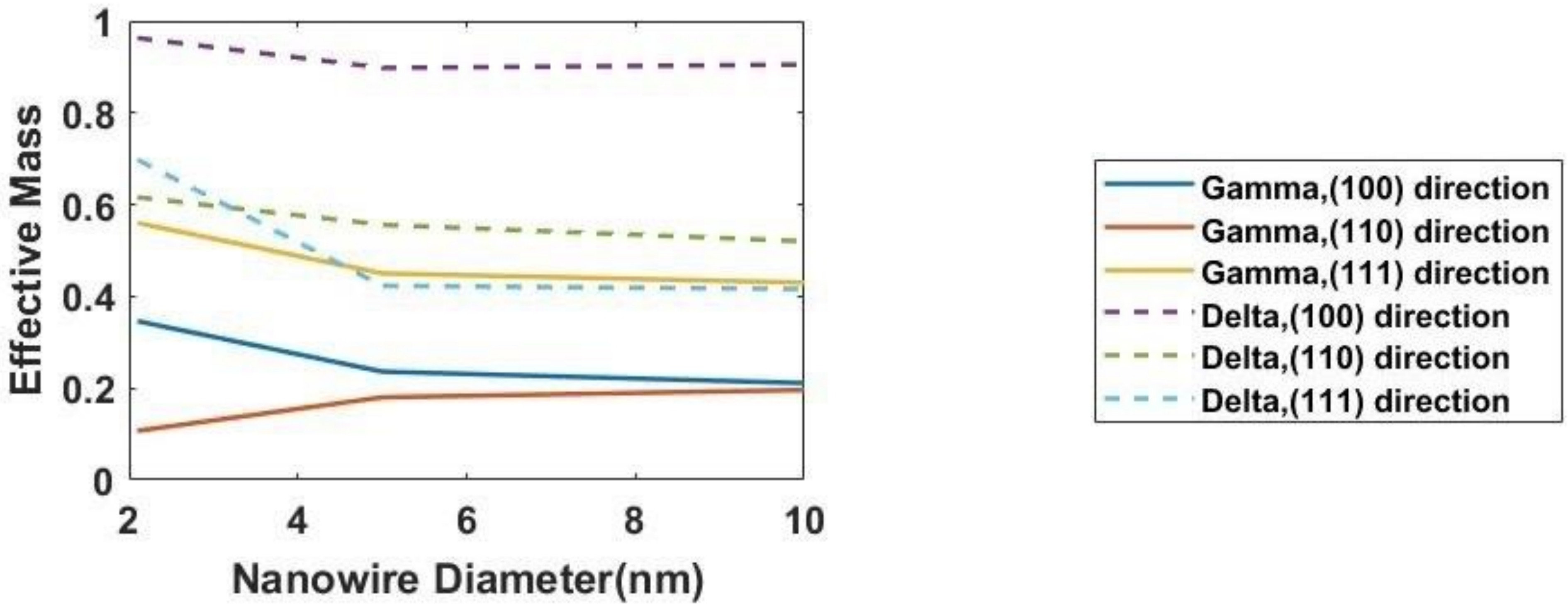
Transport direction (X): (100)

Confinement direction (Z): [010]

Tool located at: https://nanohub.org/resources/bandstrlab

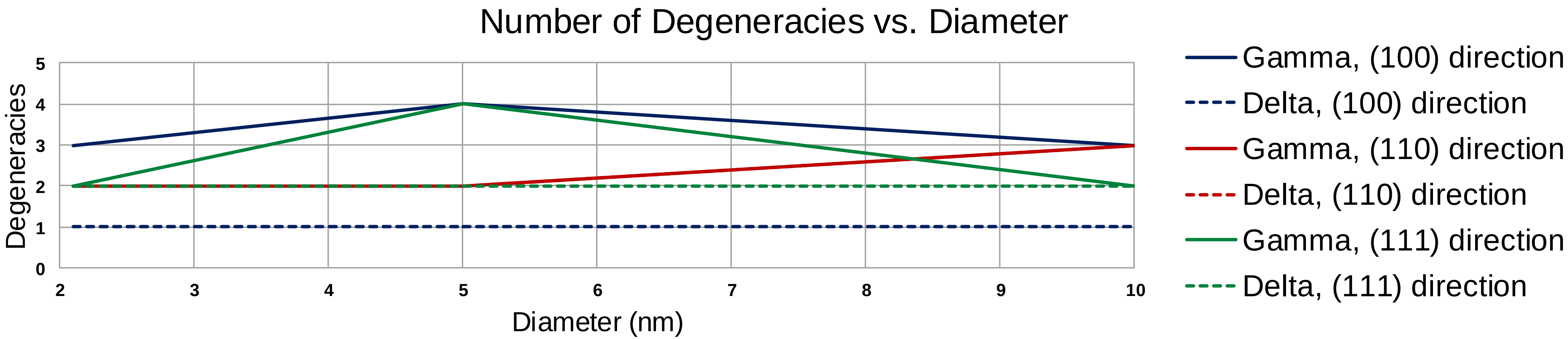


Nanowire Realistic Bandstructure (Masses)



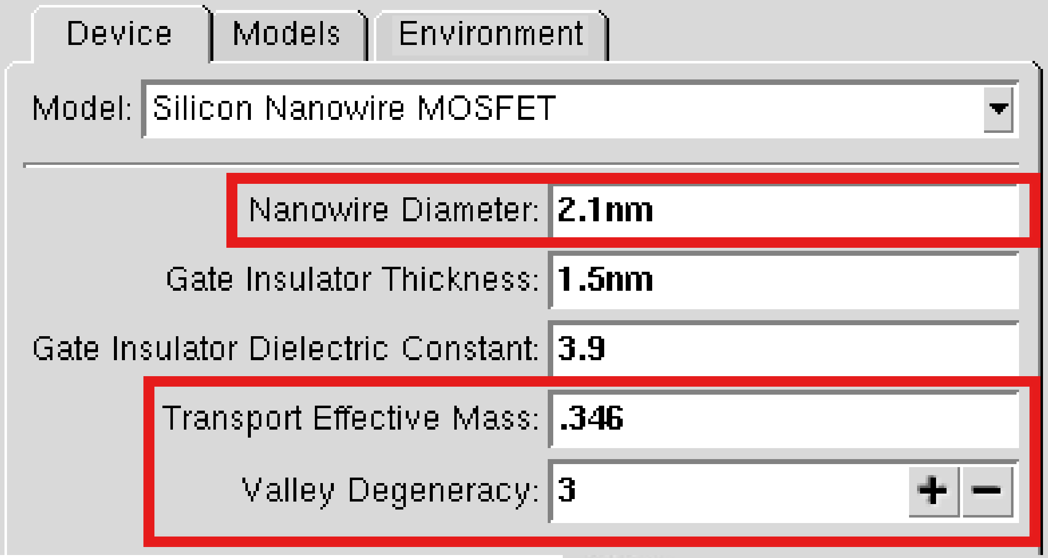
Nanowire Realistic Bandstructure (Degeneracies)

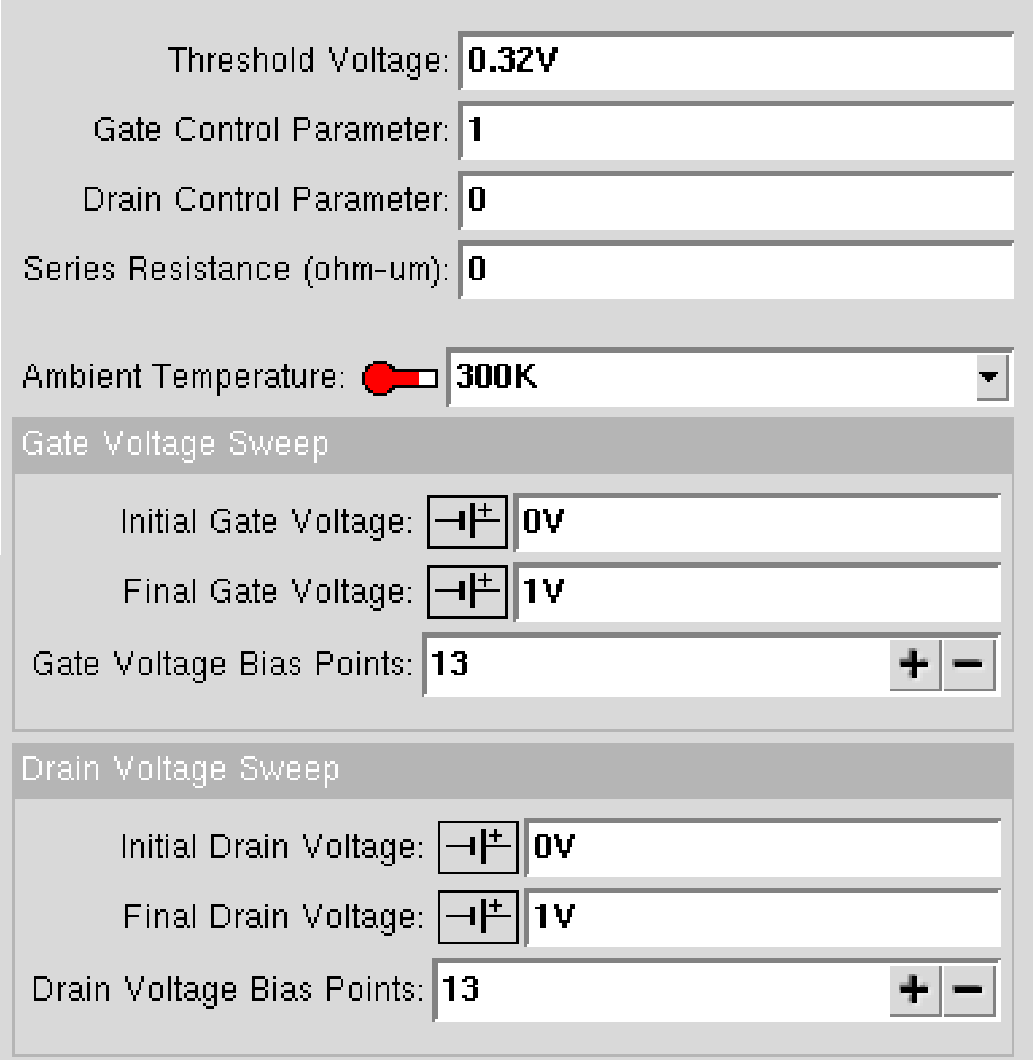
Diameter (nm)	Region	(100) direction		(110) direction		(111) direction	
		m_{eff}	Degeneracy	m_{eff}	Degeneracy	m_{eff}	Degeneracy
2.1	Gamma	0.346	3	0.107	2	0.56	2
	Delta	0.963	1	0.616	2	0.698	2
5	Gamma	0.236	4	0.180	2	0.45	4
	Delta	0.898	1	0.556	2	0.423	2
10	Gamma	0.211	3	0.196	3	0.43	2
	Delta	0.905	1	0.52	3	0.416	2

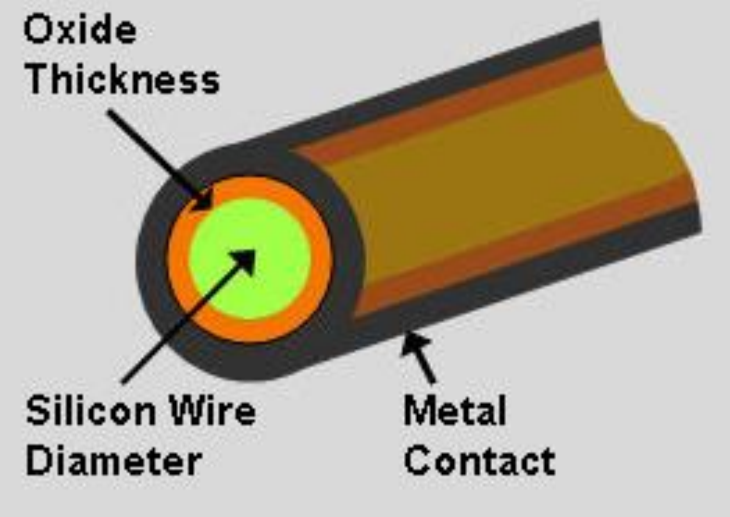


Nanowire Top-of-Barrier Transport (Inputs)

All default settings were utilized, except as where shown (red boxes mark variable inputs):

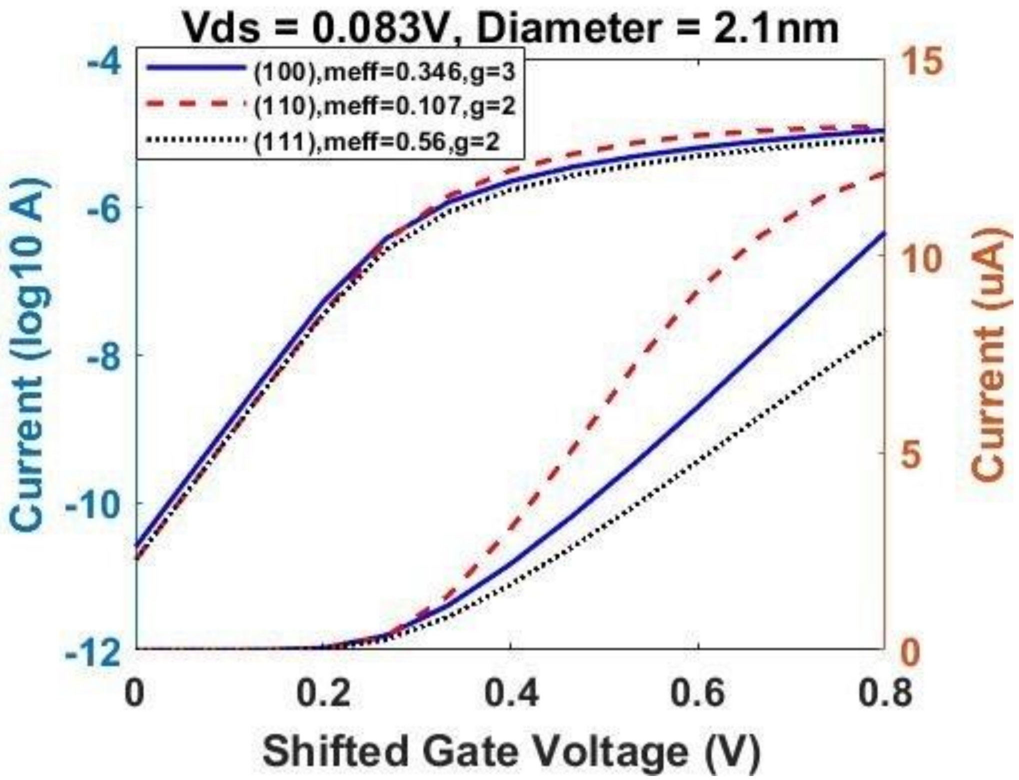


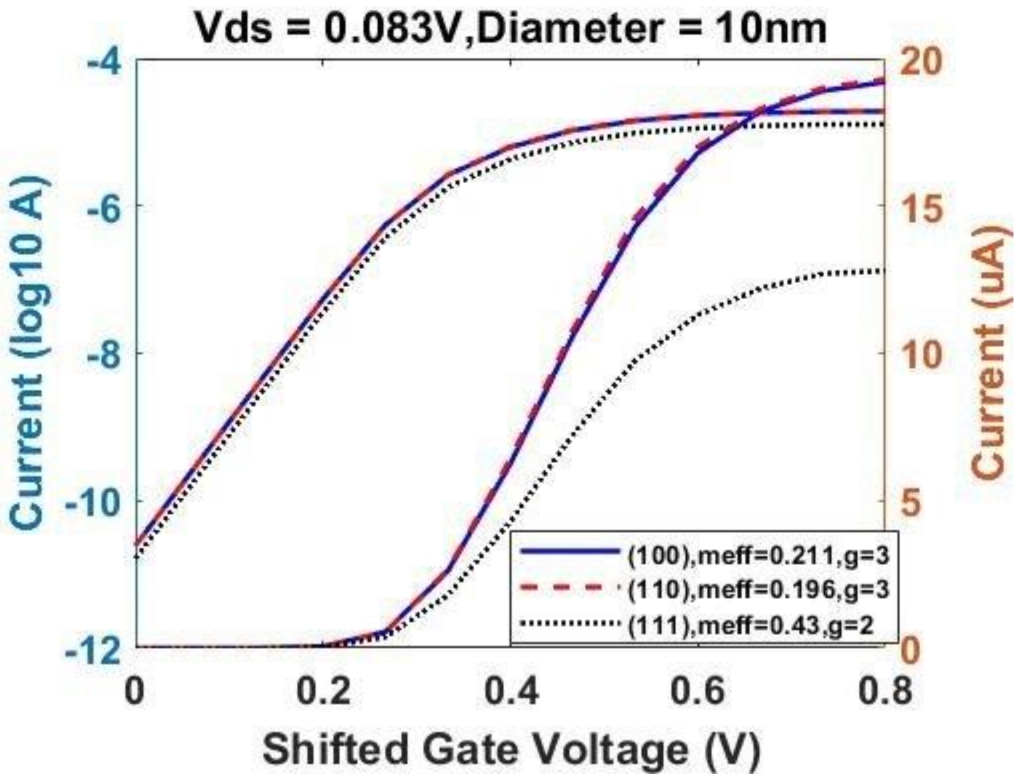




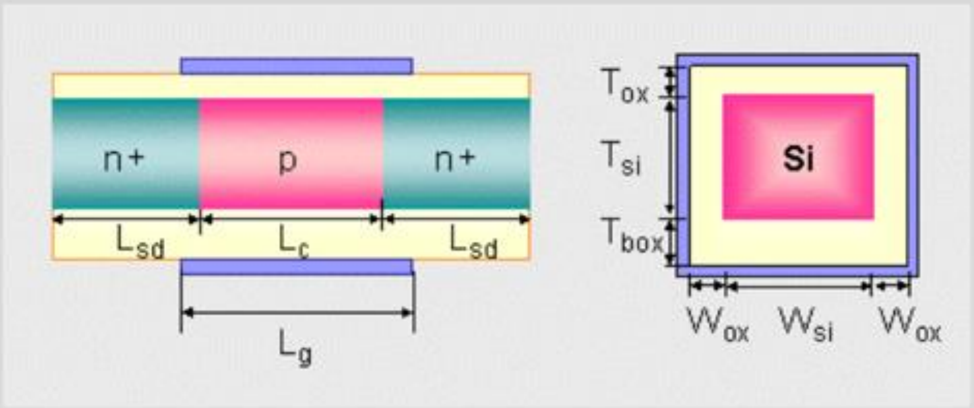
Tool located at:
https://nanohub.org/resources/fettoy

Nanowire Top-of-Barrier Transport (I-V Curves)

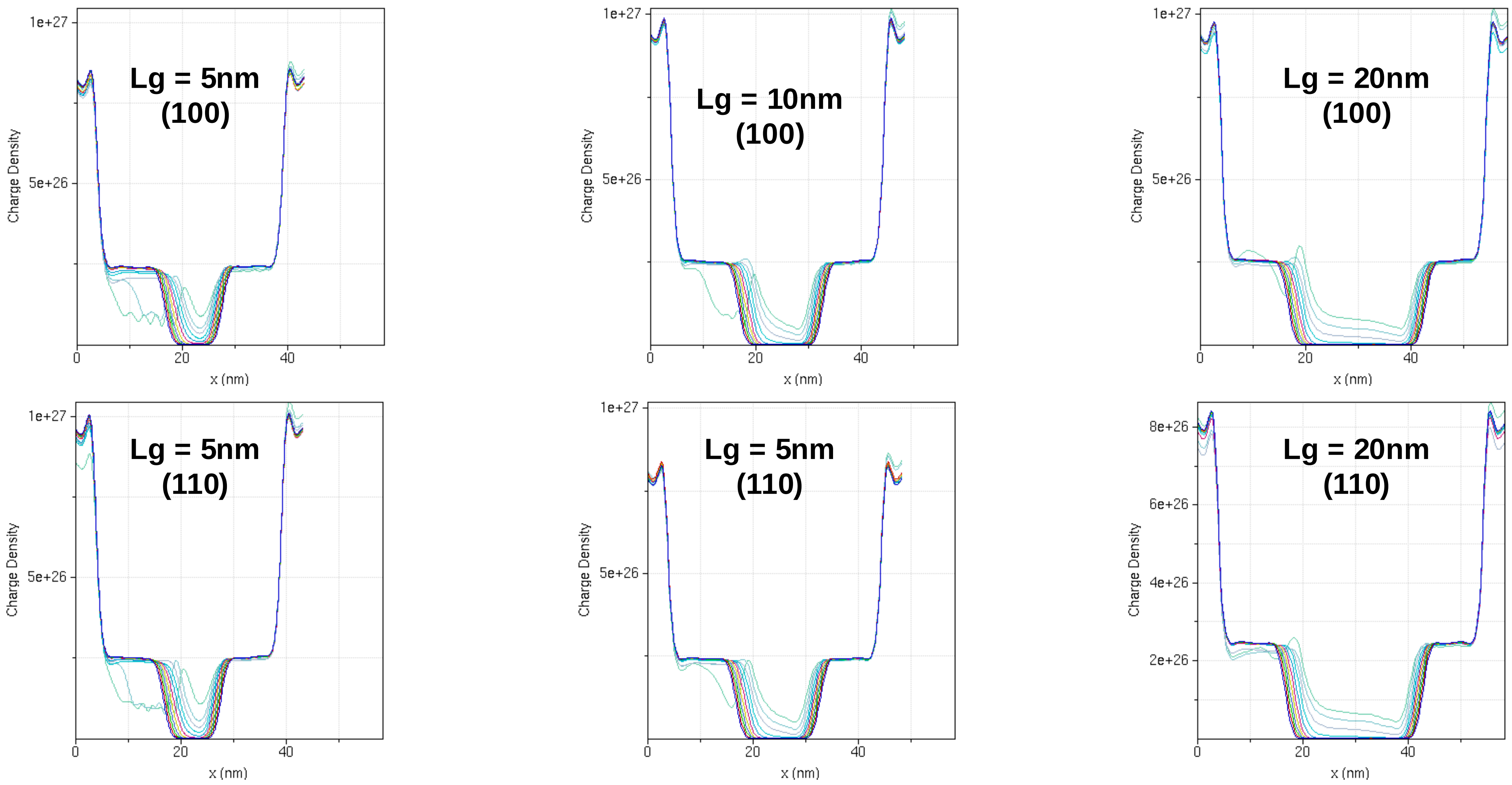




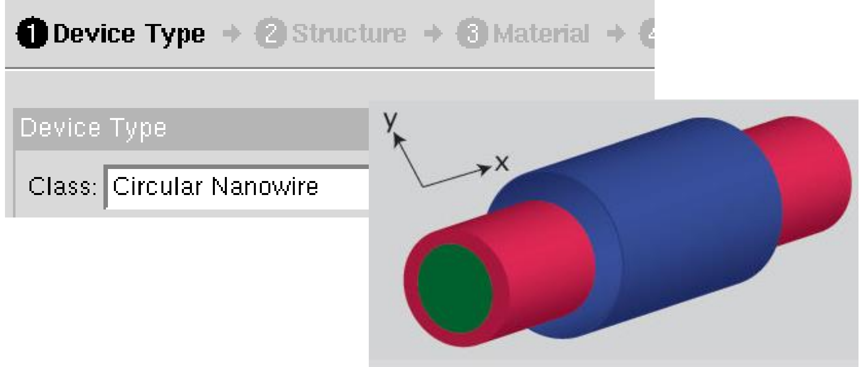
Lsd : Source/Drain Length:	20nm
Lc : Channel Length:	3nm
Lg : Gate Length:	5nm → Varied across 5nm, 10nm, 20nm
Tox : Oxide Thickness:	1nm
Tsi : Silicon Body Thickness:	3nm
Tbox : Buried Oxide Thickness:	1nm
Wox : Oxide Width:	1nm
Wsi : Silicon Body Width:	3nm

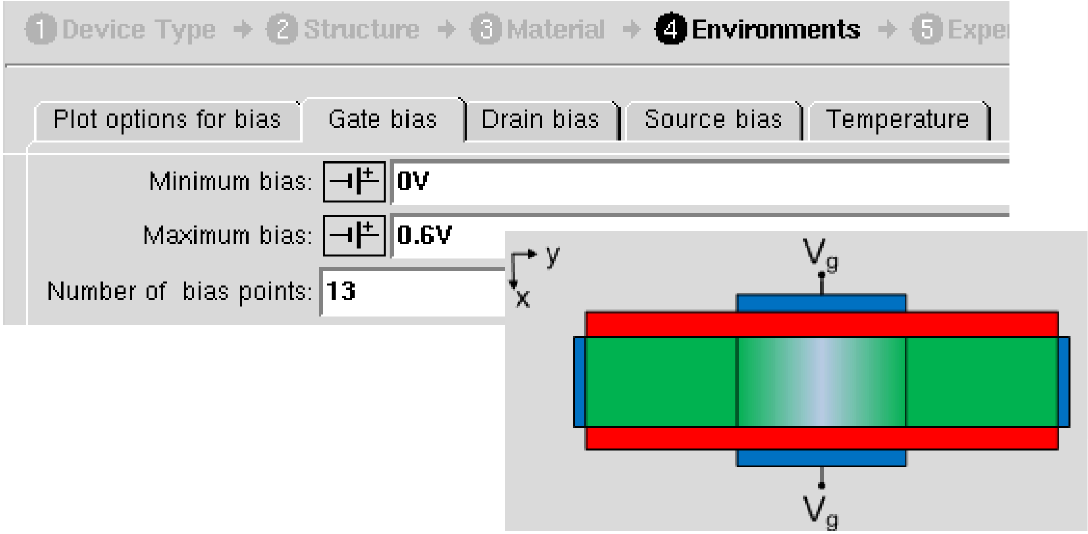


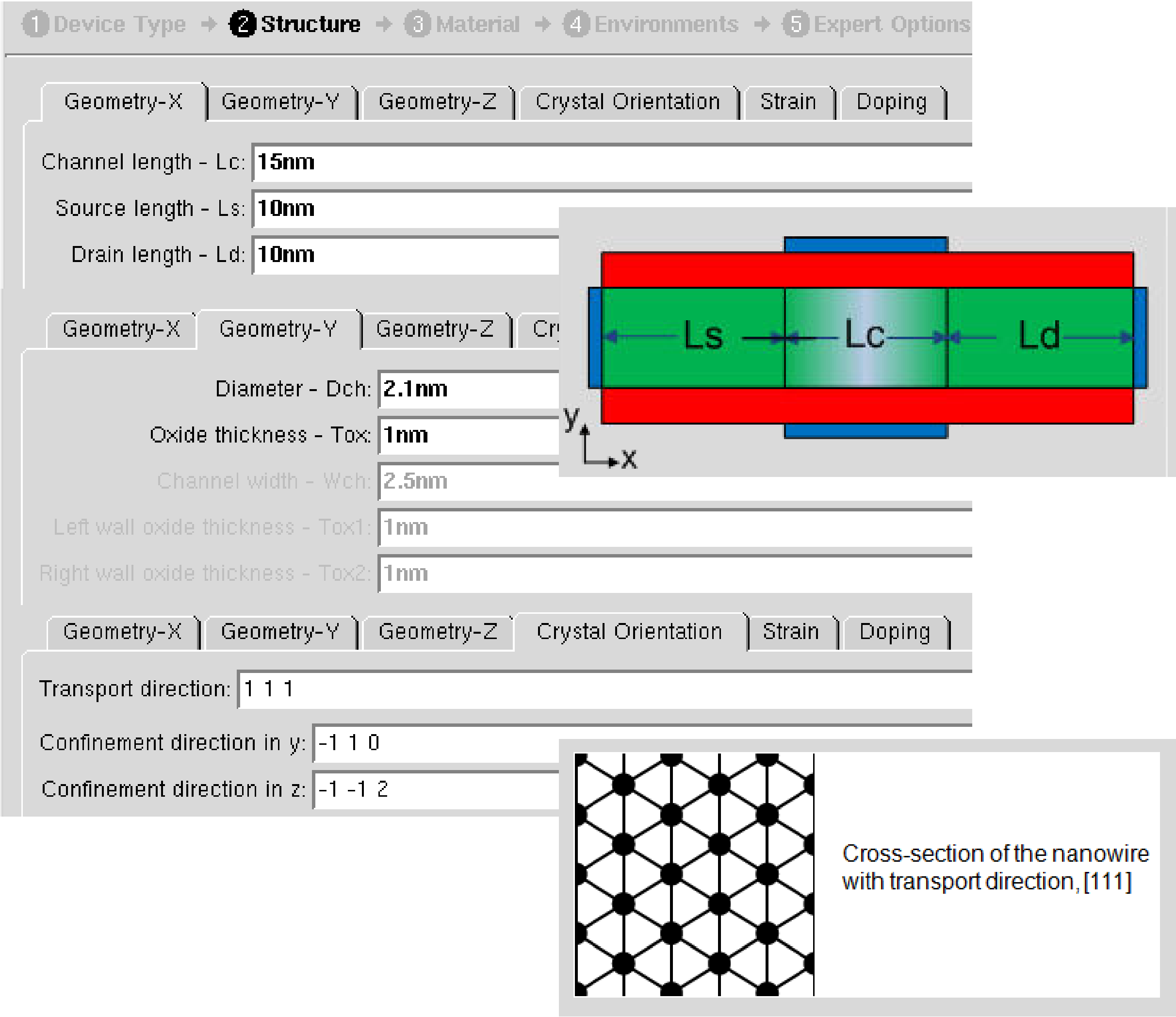
Fast Nanowire Quantum Transport (Charge Density Profiles)



Long Nanowire Quantum Transport (Inputs)

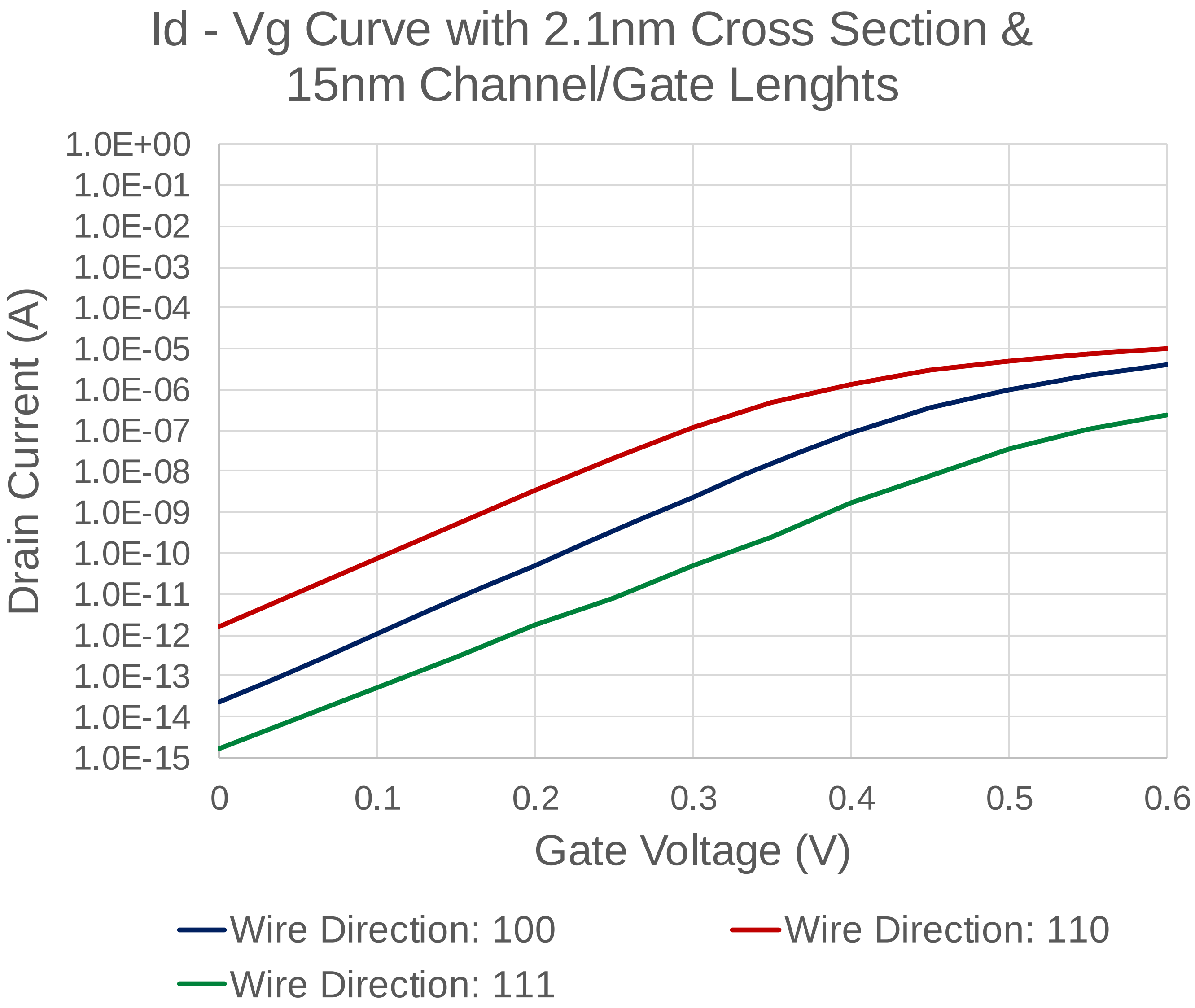






Tool located at:
https://nanohub.org/resources/omenwire

Long Nanowire Quantum Transport (Id-Vg Curve)



Critical Parameters:

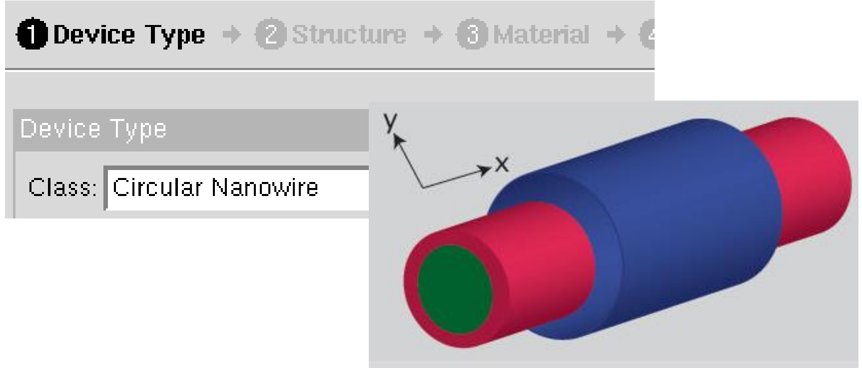
ON/OFF Current Ratio:

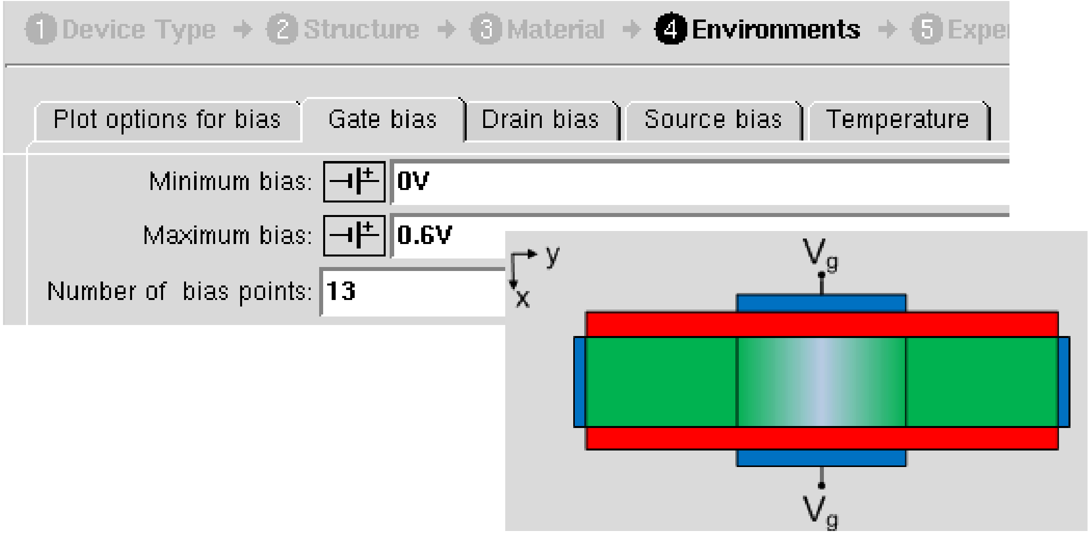
- Wire Direction 100 = 1.86×10^8
- Wire Direction 110 = 6.77×10^6
- Wire Direction 111 = 2.46×10^8

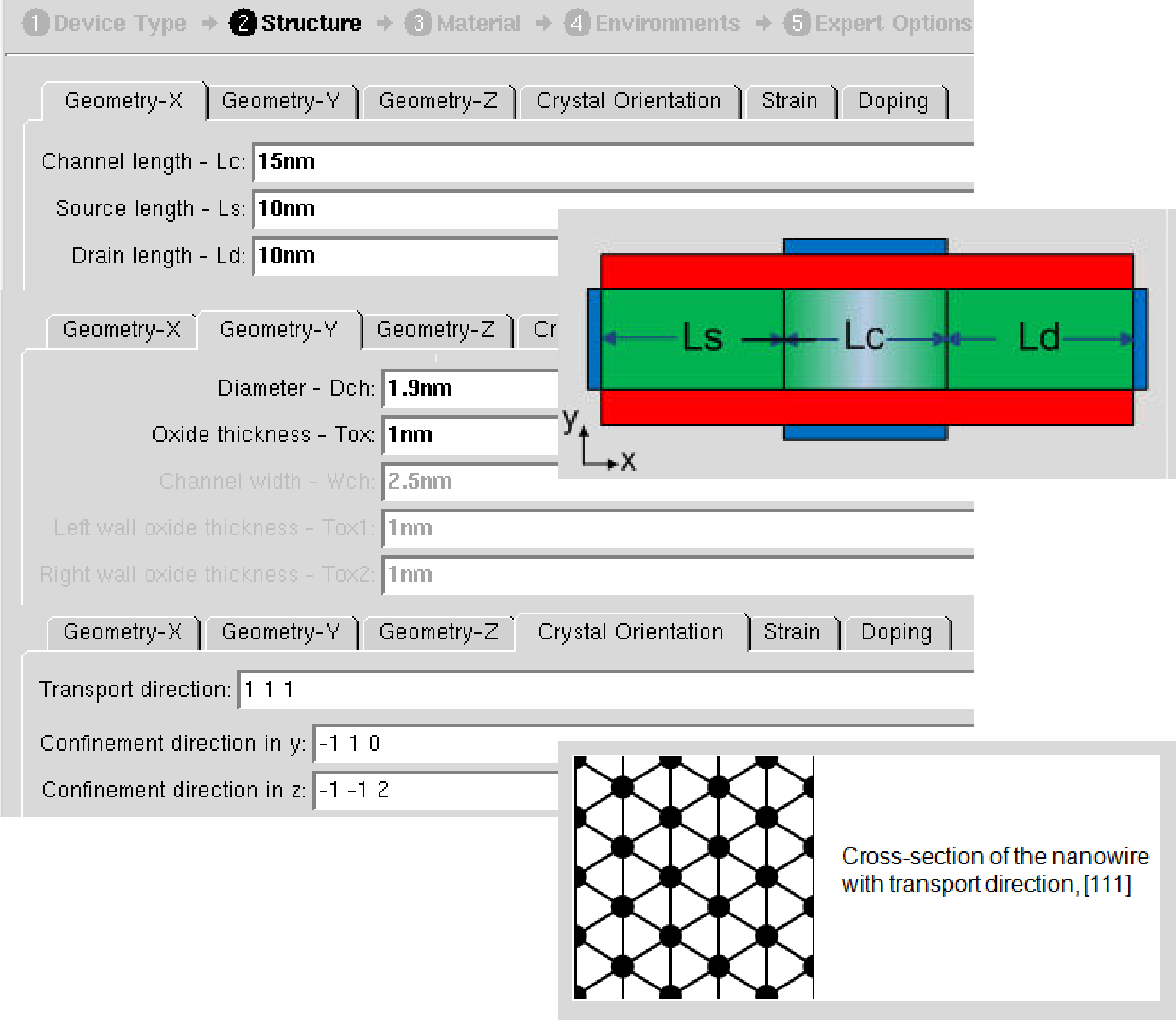
Subthreshold Swing:

- Wire Direction 100 = 59.47 mv/dec
- Wire Direction 110 = 59.87 mv/dec
- Wire Direction 111 = 60.69 mv/dec

Short Nanowire Quantum Transport (Inputs)

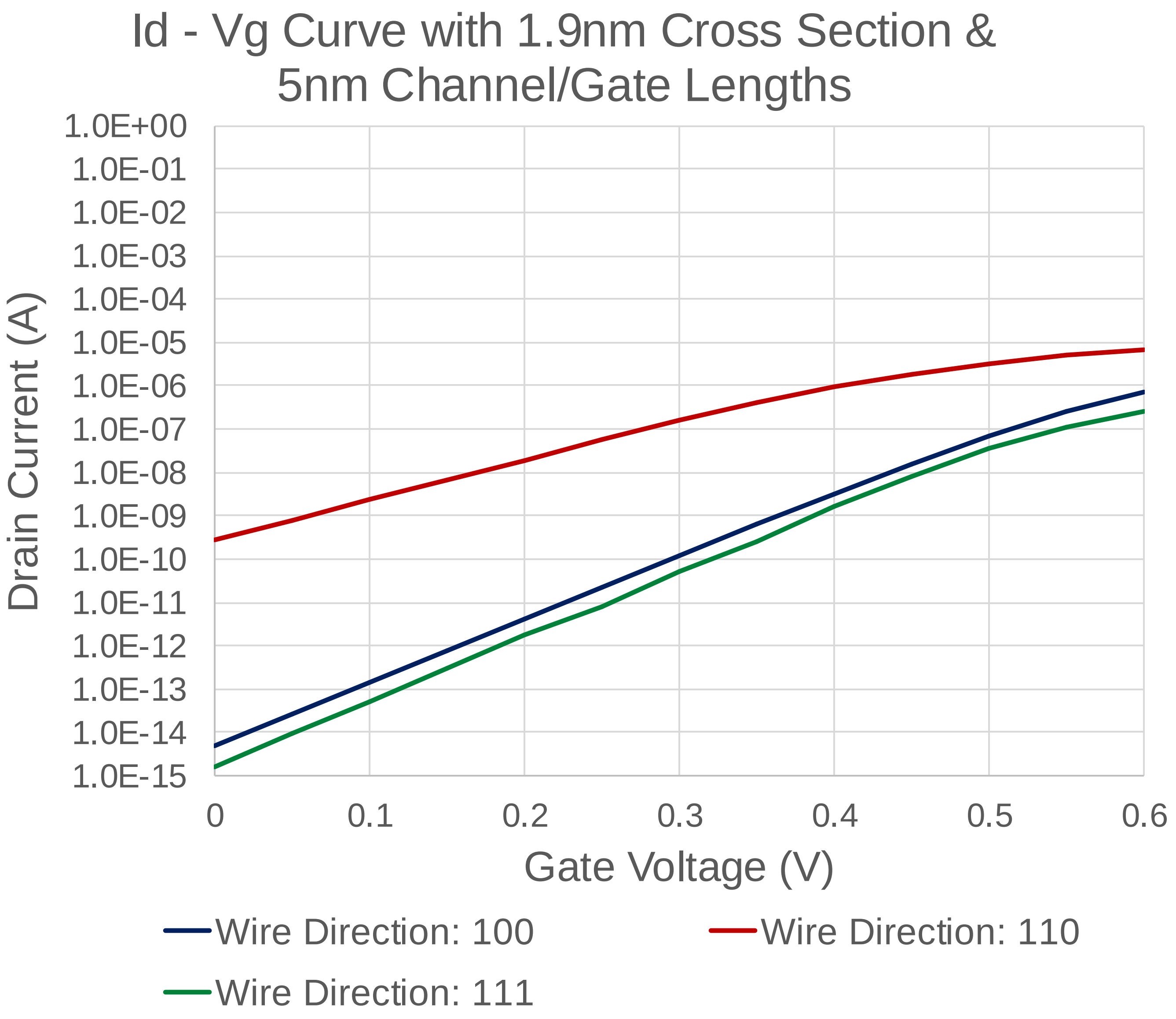






Tool located at:
https://nanohub.org/resources/omenwire

Short Nanowire Quantum Transport (Id-Vg Curve)



Critical Parameters:

ON/OFF Current Ratio:

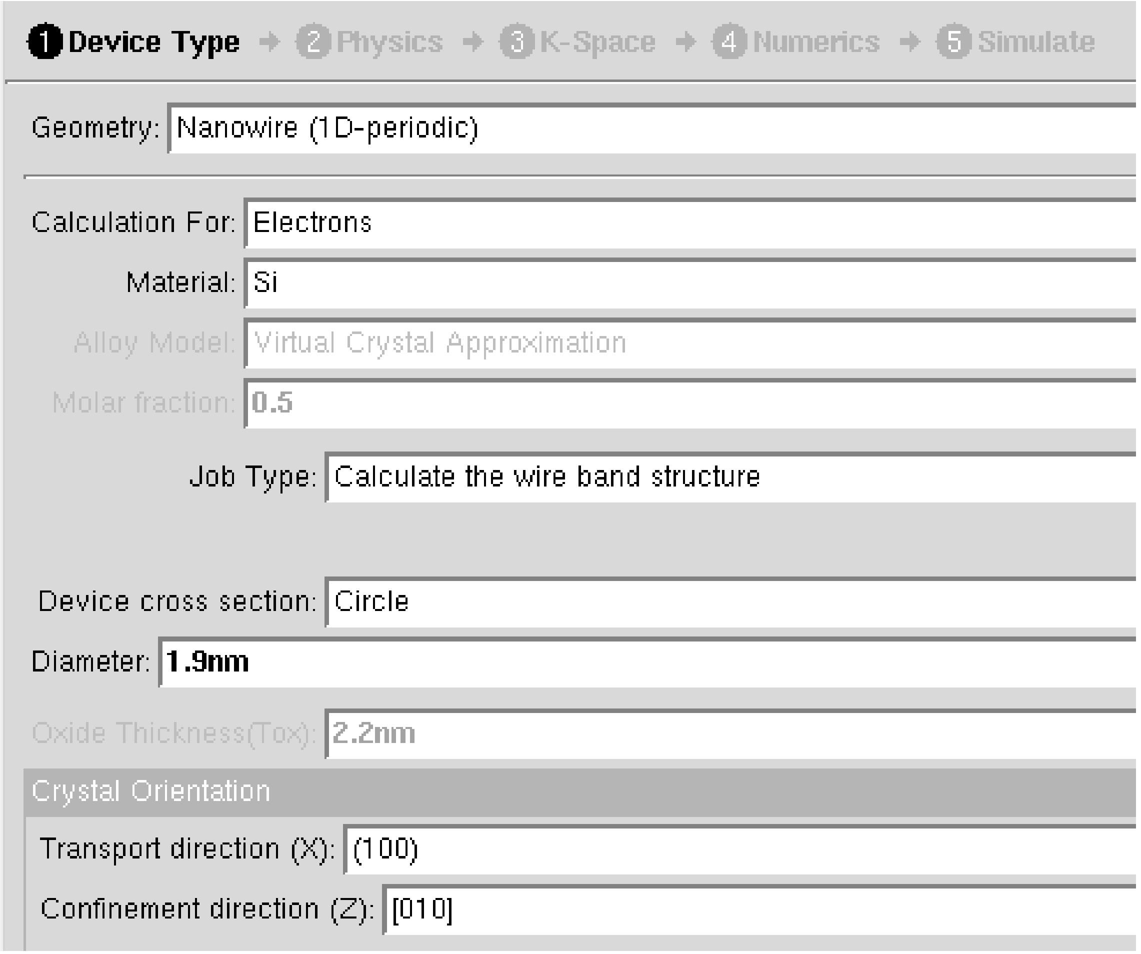
- Wire Direction 100 = 1.47×10^8
- Wire Direction 110 = 2.44×10^4
- Wire Direction 111 = 1.59×10^8

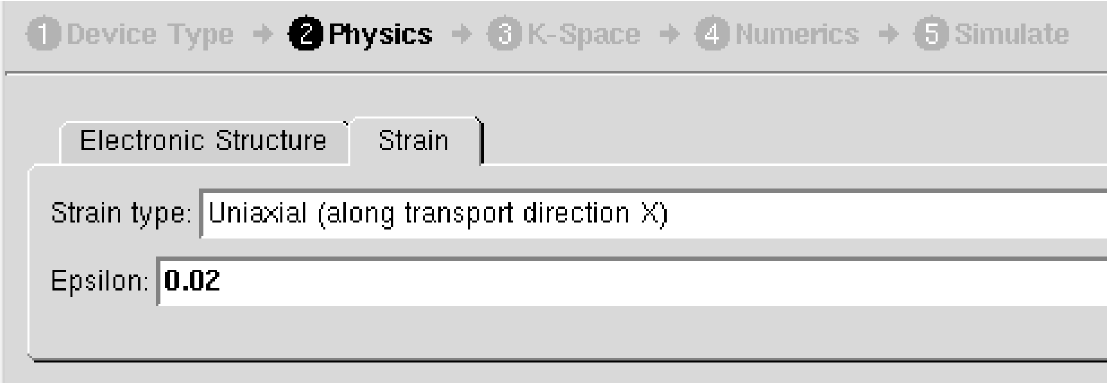
Subthreshold Swing:

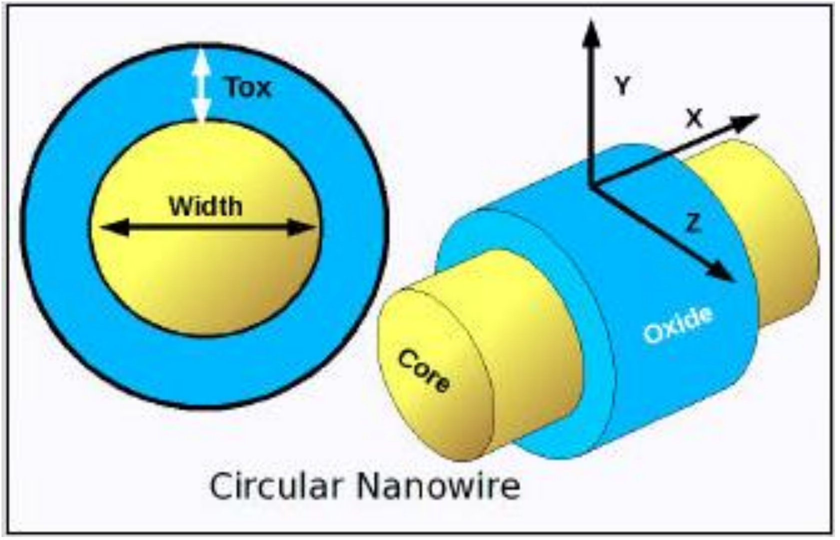
- Wire Direction 100 = 68.10 mv/dec
- Wire Direction 110 = 108.8 mv/dec
- Wire Direction 111 = 66.45 mv/dec

Nanowire Dispersion Design (Inputs)

All default settings were utilized, except as where shown:

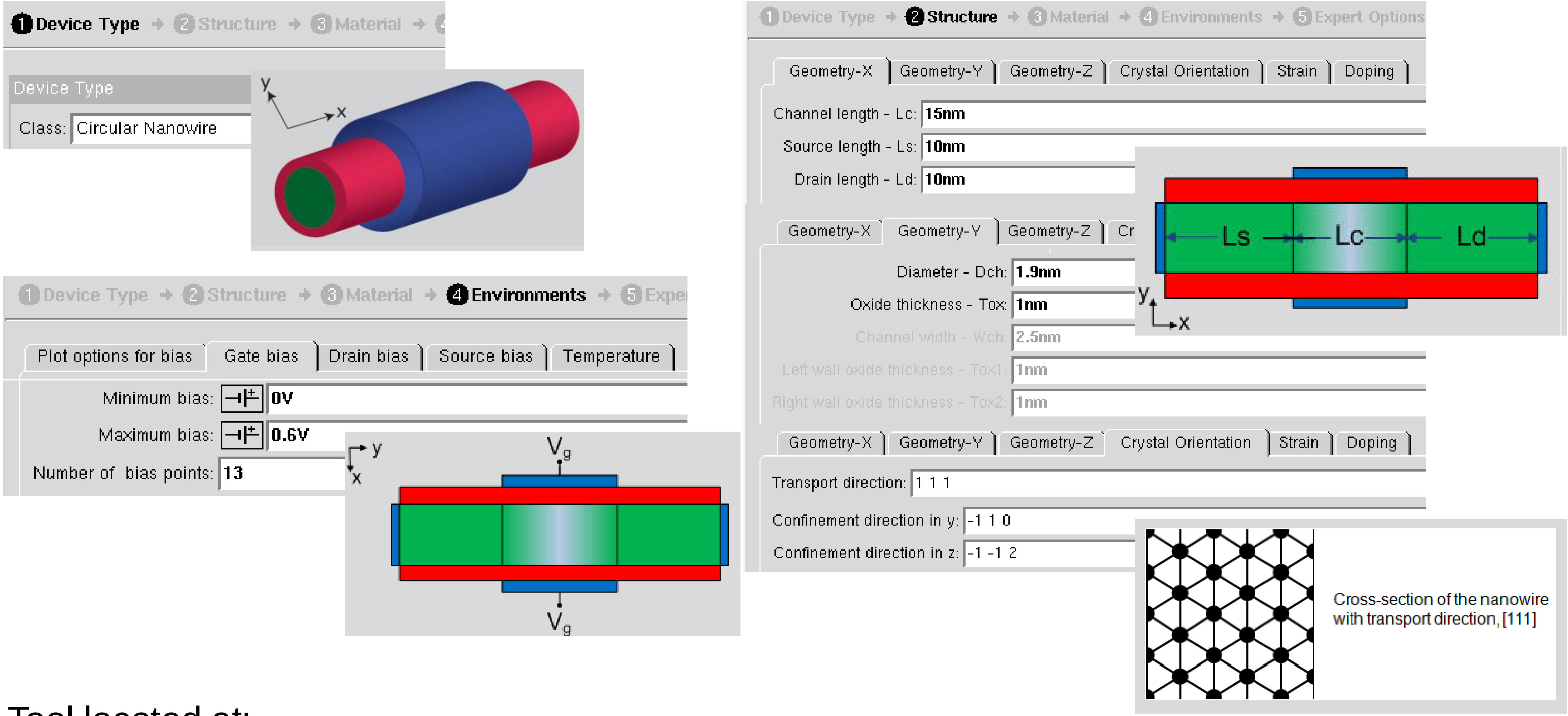






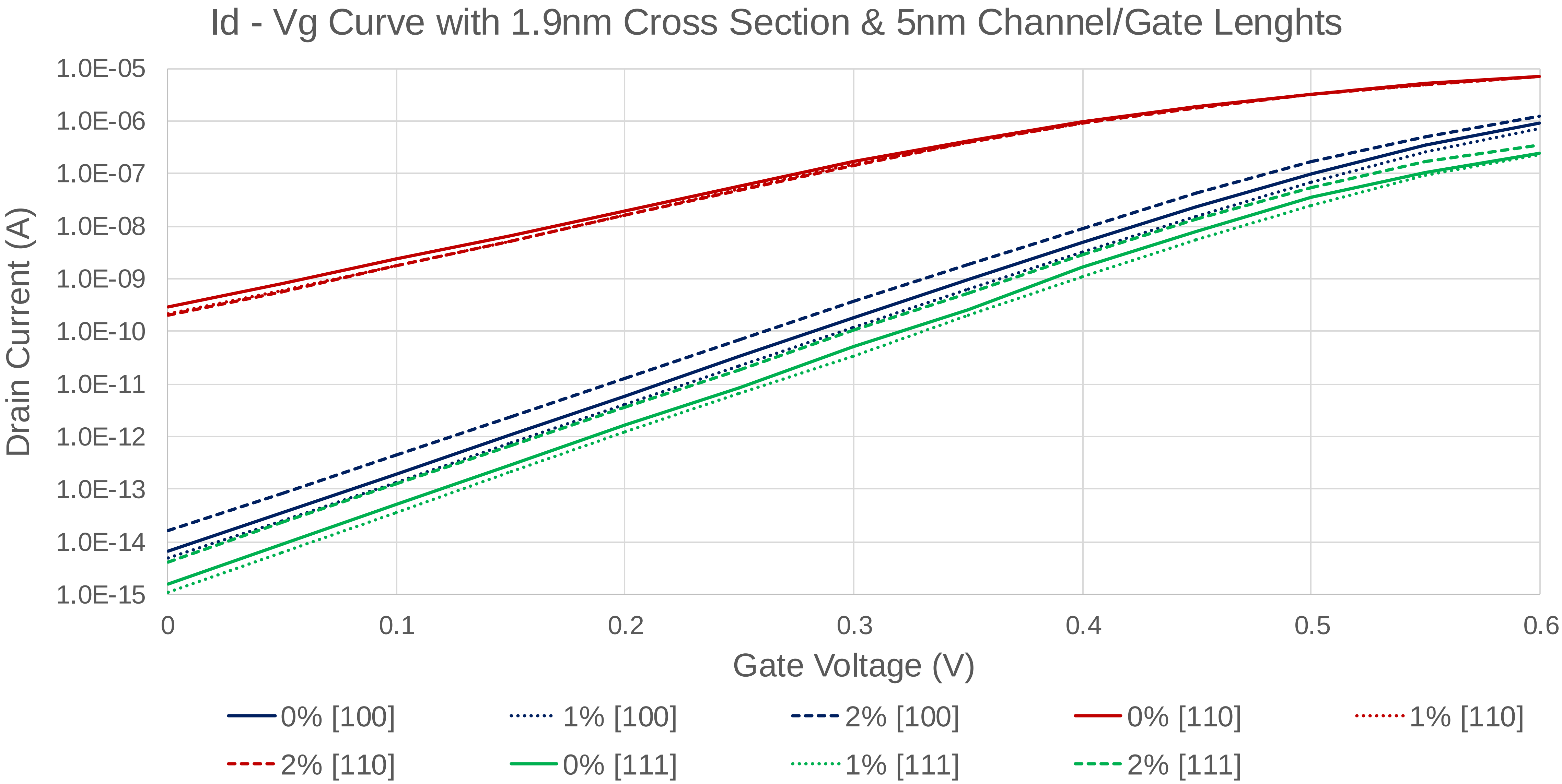
Tool located at:
https://nanohub.org/resources/bandstrlab

Optimized Nanowire Quantum Transport (Inputs)

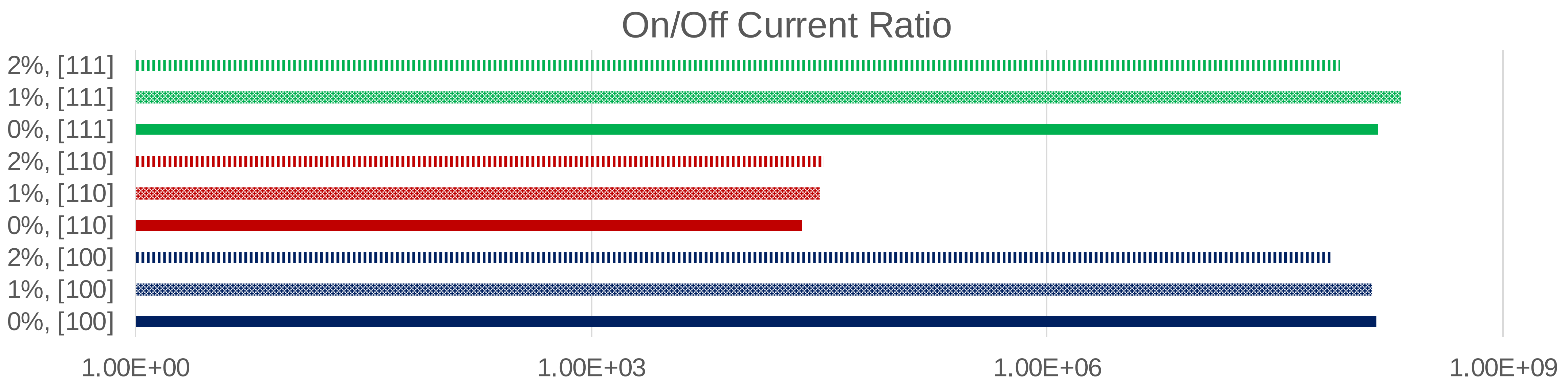


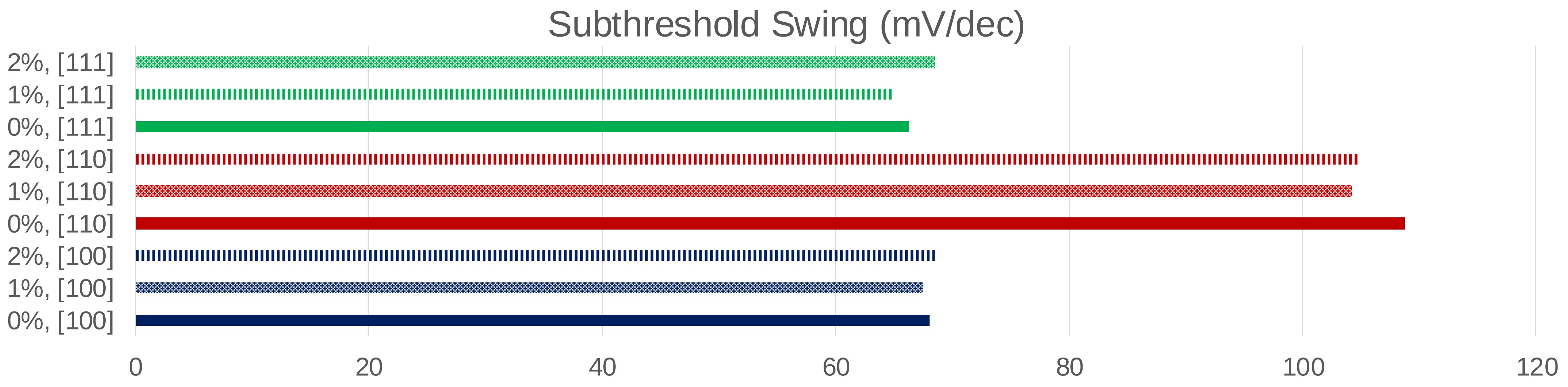
Tool located at:
https://nanohub.org/resources/omenwire

Optimized Nanowire Quantum Transport (Id-Vg Curve)



Optimized Nanowire Quantum Transport (Critical Parameters)





Hole Nanowire Bandstructure (Inputs)

All default settings were utilized, except as where shown:

1 Device Type → 2 Physics → 3 K-Space → 4 Numerics → 5 Simulate

Geometry: Nanowire (1D-periodic)

Calculation For: Electrons

Material: Si

Alloy Model: Virtual Crystal Approximation

Molar fraction: 0.5

Job Type: Calculate the wire band structure

Device cross section: Circle

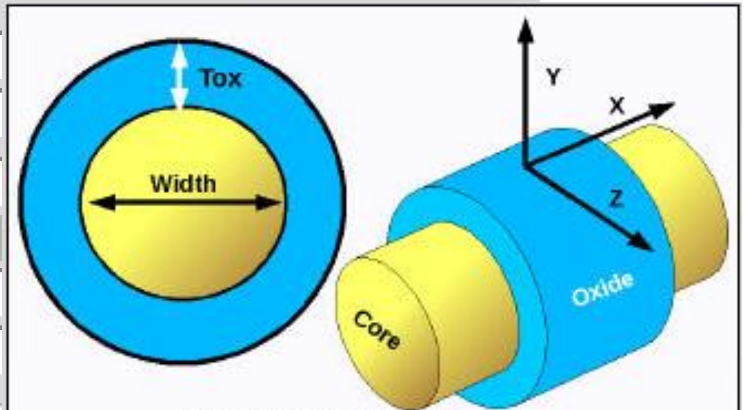
Diameter: **8nm**

Oxide Thickness(Tox): 2.2nm

Crystal Orientation

Transport direction (X): (100)

Confinement direction (Z): [010]



Circular Nanowire

1 Device Type → **2 Physics** → 3 K-Space → 4 Numerics → 5 Simulate

Electronic Structure | Strain

Tight Binding Model: sp3d5s*

Spin-Orbit Coupling: no

Dangling Bond Energy: **30eV**

Explore: Valence bands

Electronic Structure | Strain

Strain type: Uniaxial (along transport direction X)

Epsilon: **0.02**

1 Device Type → 2 Physics → 3 K-Space → **4 Numerics** → 5 Simulate

Number of k-points: **10**

Number of bands: **10**

Manual simulation venue selection: no

Simulation Venue: nanoHUB.org (local)

Tool located at:
https://nanohub.org/resources/bandstrlab

Resources

[1] W. contributors, "Work function," Wikipedia, The Free Encyclopedia., 8 February 2024. [Online]. Available: https://en.wikipedia.org/w/index.php?title=Work_function&oldid=1205050597. [Accessed 28 April 2024].

[2] W. Lee, Y. Hwangbo, J.-H. Kim, and J.-H. Ahn, “Mobility enhancement of strained Si transistors by transfer printing on plastic substrates,” *NPG Asia Materials*, vol. 8, no. 3, pp. e256–e256, Mar. 2016, doi: https://doi.org/10.1038/am.2016.31.

[3] “Strained Transistors - REFERENCE PMOS-strained,” *www.intel.com*. https://www.intel.com/pressroom/kits/advancedtech/doodle/ref_strain/strain.htm

[4] Y. Chen *et al.*, “Mobility Enhancement of Strained MoS_2 Transistor on Flat Substrate,” *ACS nano*, vol. 17, no. 15, pp. 14954–14962, Jul. 2023, doi: https://doi.org/10.1021/acsnano.3c03626.

[5] K. Mistry *et al.*, “Delaying forever: Uniaxial strained silicon transistors in a 90nm CMOS technology,” *IEEE Xplore*, Jun. 01, 2004. https://ieeexplore.ieee.org/document/1345387